OR6515HDC

High Efficiency, 15A Synchronous Step Up Regulator with Accurate Output Current Limit

General Description

The OR6515HDC develops a high efficiency synchronous Boost regulator with programmable output current limit.The device adopts adaptive constant off time and current mode control. The integrated low $R_{DS(ON)}$switches minimize the conduction loss.

The OR6515HDC features cycle-by-cycle peak current limit, output short circuit protection and true shutdown. The device also provides enable control and power good indicator for system sequence control. Low output voltage ripple and small external inductor and capacitor size are achieved with programmable pseudo-constant frequency.

Features

- Input Range: 4.5-30V
- Programmable Pseudo-constant Frequency
- Low $R_{DS(ON)}$ Internal Switch
  Main FET: 16mΩ
  Rectified FET: 18mΩ
  Disconnection FET: 18mΩ
- True Shutdown Function
- Programmable Output Current Limit
- Internal Soft-start Limits the Inrush Current
- Input Voltage UVLO
- Over Temperature Protection
- Over Voltage Protection
- Output Short Circuit Protection
- Minimum ON Time: 100ns typical
- Minimum OFF Time: 120ns typical
- RoHS Compliant and Halogen Free
- Compact Package:QFN4×4-18

Ordering Information

OR6515□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
OR6515HDC	QFN4×4-18	----

Applications

- Power Bank
- High Power AP

Typical Applications

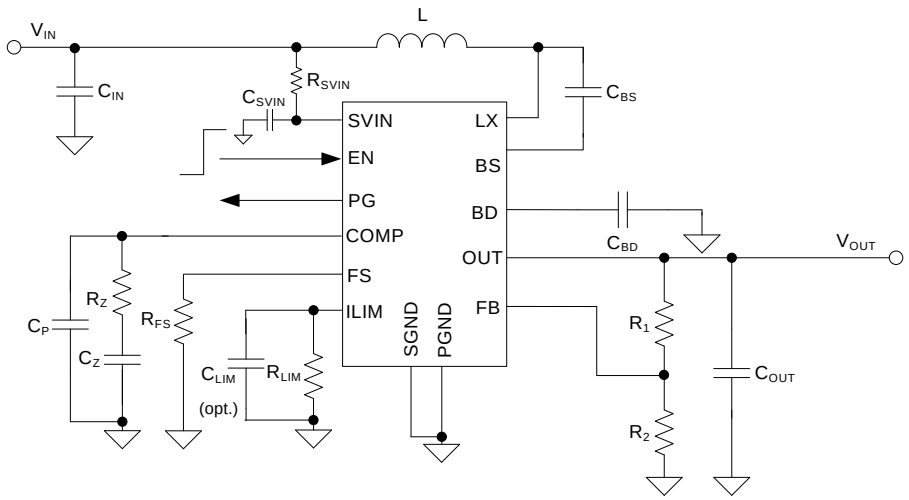
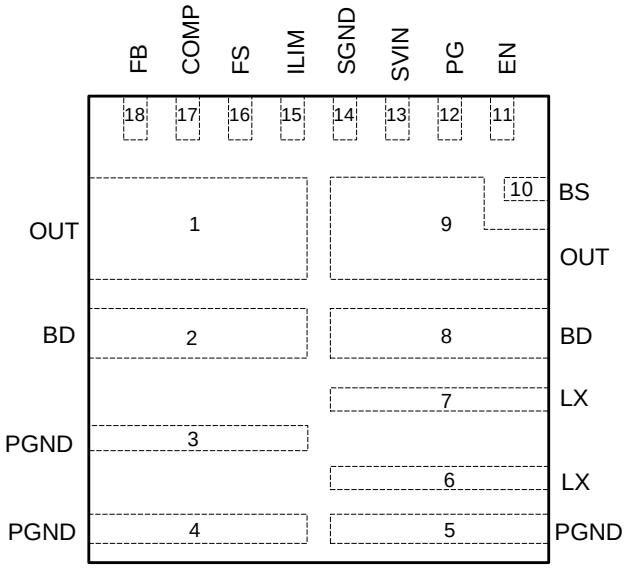


Figure1. Schematic Diagram

Pinout (top view)



(QFN4×4-18)

Top mark: **AVZ*xyz*** (Device code: AVZ, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
OUT	1,9	The Boost converter output pin.
BD	2,8	Connect to the Drain of internal Disconnect FET. Bypass at least a 4.7μF ceramic capacitor to PGND.
PGND	3,4,5	Power ground pin.
LX	6,7	Inductor node. Connect an inductor from power input to the LX pin.
BS	10	Boot-strap pin. Supply Rectified FET's gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
EN	11	Enable control. Pull high to turn on the IC. Do not leave it floating.
PG	12	Power good indicator. Open drain output, pull low when the output < 90% of regulation voltage, high impendence otherwise.
SVIN	13	IC power supply pin. Decouple this pin to the SGND pin with a 2.2μF ceramic capacitor.
SGND	14	Signal ground pin.
ILIM	15	Output current limit program pin. Connect a resistor R_{LIM} from this pin to SGND to program output current limitation threshold. $I_{LIM}(A)=30(V)/ R_{LIM}(k\Omega)$
FS	16	Switching frequency setting pin. Connect a resistor from this pin to ground to program the switching frequency. $f_{SW}(kHz)=1.4\times10^6/R_{FS}(\Omega)^{0.645}$.
COMP	17	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
FB	18	Feedback pin. Connect to the center of resistor voltage divider to program the output voltage: $V_{OUT}=1V\times(R_1/R_2+1)$

Block Diagram

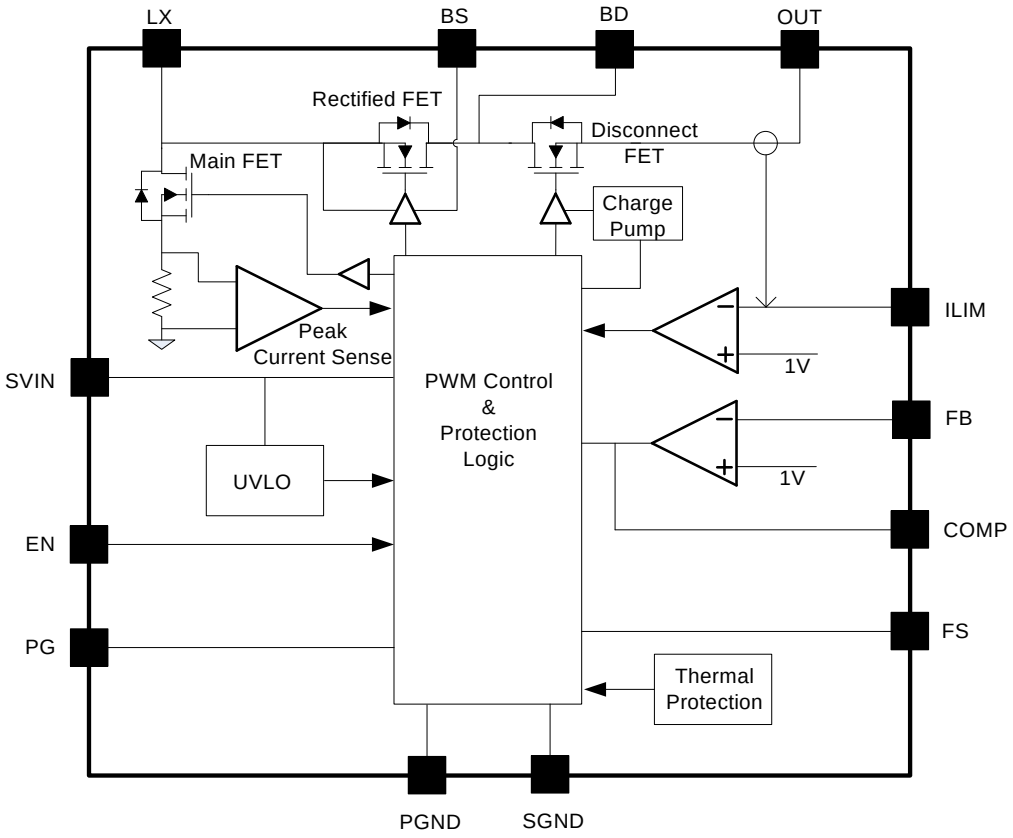


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

SVIN, LX, EN, ILIM, OUT, BD, FS, PG, COMP Voltage ---------- -0.3V to 33V
FB Voltage---------- -0.3V to 4V
BS-LX Voltage ---------- -0.3V to 4V
Dynamic LX Voltage in 10ns Duration ---------- -3.5V to 36V
Power Dissipation, P_D @ T_A = 25°C QFN4×4-18----------3.4W
Package Thermal Resistance (Note 2)
θ_{JA} ----------30°C/W
θ_{JC} ----------3.2°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

SVIN ---------- 4.5V to 30V
Junction Temperature Range ---------- - 40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =5V, V_{OUT}=12V, I_{OUT}=100mA, T_A = 25°C, unless otherwise specified)

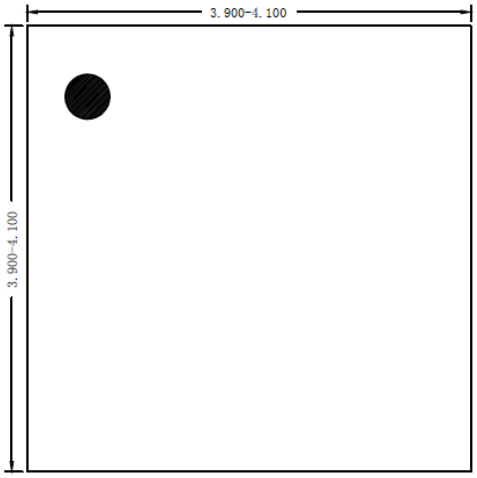
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		30	V
Input UVLO Threshold	V_{UVLO}			4	4.35	V
UVLO Hysteresis	V_{HYS}			0.2		V
Quiescent Current	I_Q	V_{OUT}=13V			230	μA
Shutdown Current	I_{SHDN}	EN=0			5	μA
Feedback Reference Voltage	V_{REF}		0.985	1	1.015	V
FB Input Current	I_{FB}	V_{FB}=2V	-50		50	nA
Main FET RON	$R_{DS(ON),M}$			16		mΩ
Rectified FET RON	$R_{DS(ON),R}$			18		mΩ
Disconnect FET RON	$R_{DS(ON),D}$			18		mΩ
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Min ON Time	$t_{ON,MIN}$			100		ns
Min OFF Time	$t_{OFF,MIN}$			120		ns
Switching Frequency	f_{SW}	R_{FS}=390kΩ		345		kHz
Switching Frequency Programmable Range			200		1000	kHz
Power Good Threshold	V_{PG}	V_{FB} Rising (Good)		90		%V_{REF}
Power Good Hysteresis	$V_{PG,HYS}$			2.5		%V_{REF}
Power Good Delay	$t_{PG,RISING}$	Low to high		40		μs
	$t_{PG,FALLING}$	High to low		30		μs
Power Good Output Low	V_{PGL}	I_{PG}=4mA		0.15		V
BD Over Voltage Threshold	V_{OVP}	V_{FB} Rising	31			V
BD Over Voltage Hysteresis	$V_{OVP,HYS}$			0.5		V
BD OVP Delay	$t_{OVP,DLY}$			5		μs
Output Under Voltage Protection Threshold	V_{UVP}			2		V
Output UVP Delay	$t_{UVP, DLY}$			2		us
Hic-cup ON Time	$t_{UVP, ON}$			2		ms
Hic-cup OFF Time	$t_{UVP, OFF}$			12		ms
Main N-FET Current Limit	$I_{LIM,PEAK}$		15		21	A
Output Current Limit Programmable Range	$I_{LIM,OUT}$		1		4	A
Output Current Limit Accuracy	$I_{LMT,ACC}$		-25		25	%
Output Current Limit Reference Voltage	V_{LIM}			1		V
Error Amplifier Trans-conductance	g_m			100		μS
Current Sense Gain	R_i			75		mΩ
Thermal Shutdown Temperature	T_{SD}			150		˚C
Thermal Shutdown Hysteresis	T_{HYS}			15		˚C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Orange Evaluation Board.

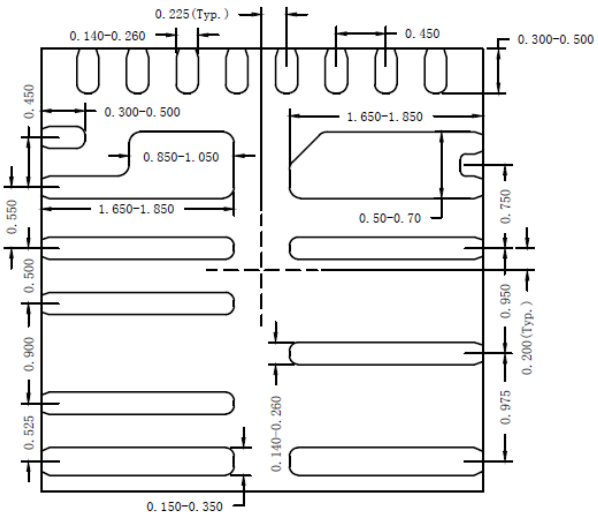
Note 3: The device is not guaranteed to function outside its operating conditions.

QFN4×4-18 Package Outline Drawing

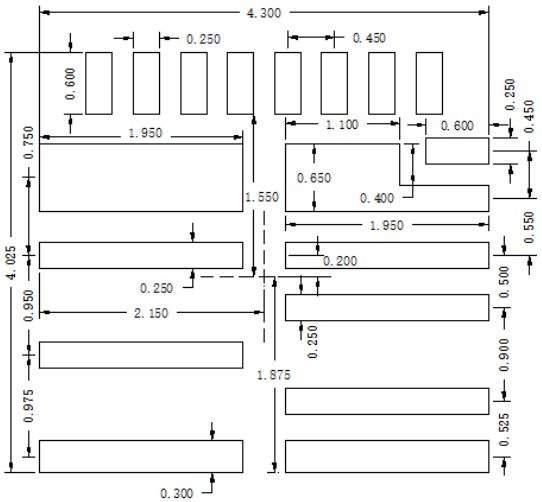


Top View

Side View



Bottom View



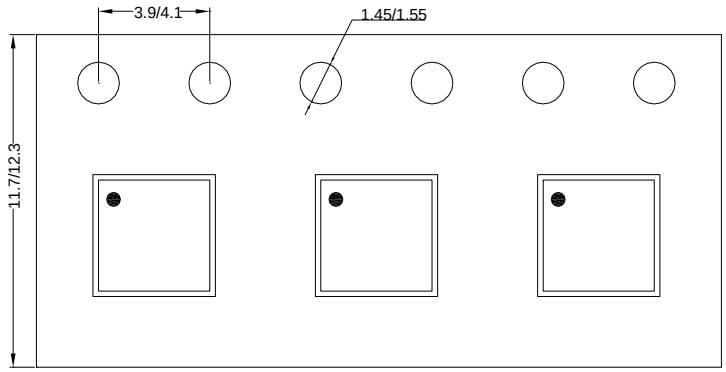
Recommended PCB layout (Reference only)

Notes: All dimensions in millimeter and exclude mold flash & metal burr;
The center of PCB diagram refers to chip body center.

Taping & Reel Specification

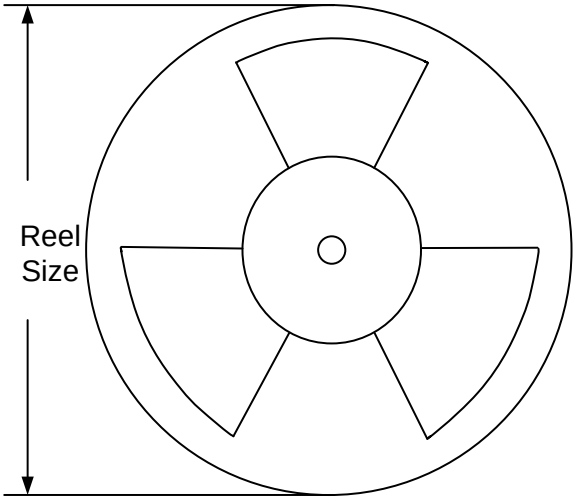
1. Taping orientation

QFN4×4



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

3. Others: NA