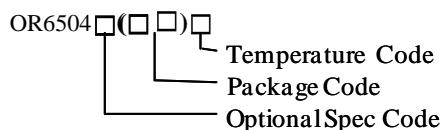




## General Description

The OR6504CBC is a high efficiency, current-mode control Boost regulator. The device integrates a 120mΩ low  $R_{DS(ON)}$  N-channel MOSFET for high efficiency. The fixed 1MH switching frequency and internal compensation reduce external components size and count. The build-in internal soft start circuitry minimizes the inrush current at start-up. The OR6504CBC is available in compact DFN3×3-10 package.

## Ordering Information



Ordering Number	Package type	Note
OR6504CBC	DFN3×3-10	4A

## Features

- Wide input range: 3-33V
- Maximum output voltage: 33V
- 1MHz switching frequency
- Integrated 120 mΩ  $R_{DS(ON)}$  switch with 4A peak current capability
- Internal soft-start
- 0.6V±2% reference voltage
- Cycle by cycle peak current limit
- Over temperature protection
- RoHS Compliant and Halogen Free
- Compact package: DFN3×3-10

## Applications

- Portable Device
- Battery Powered System
- Networking cards powered from PCI or PCI-express slots

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## Typical Applications

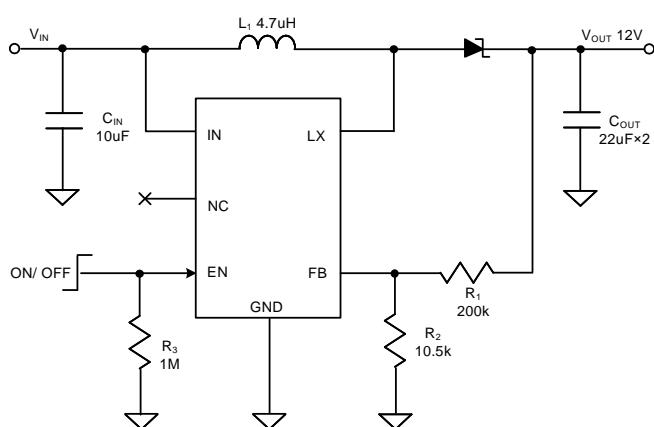


Figure 1. Schematic Diagram

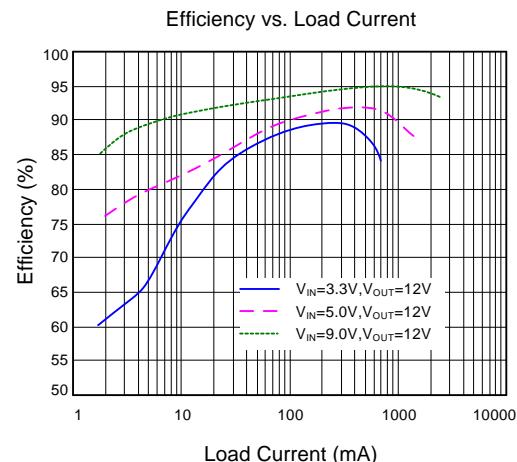
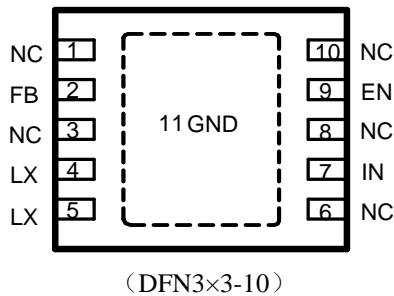


Figure 2. Efficiency vs. Load Current



## Pinout (top view)



**Top Mark: VIxyz** (Device code: VI, x=year code, y=week code, z= lot number code)

Pin Name	Pin Number	Pin Description
IN	7	Input pin. Decouple this pin to GND pin with 1uF ceramic cap.
GND	11	Ground pin
LX	4,5	Inductor node. Connect an inductor between IN pin and LX pin.
FB	2	Feedback pin. Connect a resistor R1 between V <sub>OUT</sub> and FB, and a resistor R2 between FB and GND to program the output voltage: V <sub>OUT</sub> =0.6V*(R1/R2+1).
EN	9	Enable control. High to turn on the part. Don't leave it floated.
NC	1,3,6,8,10	No connection.

## Absolute Maximum Ratings (Note 1)

LX, IN, EN ----- -0.3V to 36V

FB ----- -0.3V to 4V

Power Dissipation, P<sub>D</sub> @ T<sub>A</sub> = 25°C DFN3x3-10 ----- 2.6W

Package Thermal Resistance (Note 2)

θ<sub>JA</sub> ----- 38°C/W

θ<sub>JC</sub> ----- 8°C/W

Junction Temperature Range ----- -40 to 150°C

Lead Temperature (Soldering, 10 sec.) ----- 260°C

Storage Temperature Range ----- -65°C to 150°C

Dynamic LX voltage in 50ns duration ----- IN+3V to GND-4V

## Recommended Operating Conditions (Note 3)

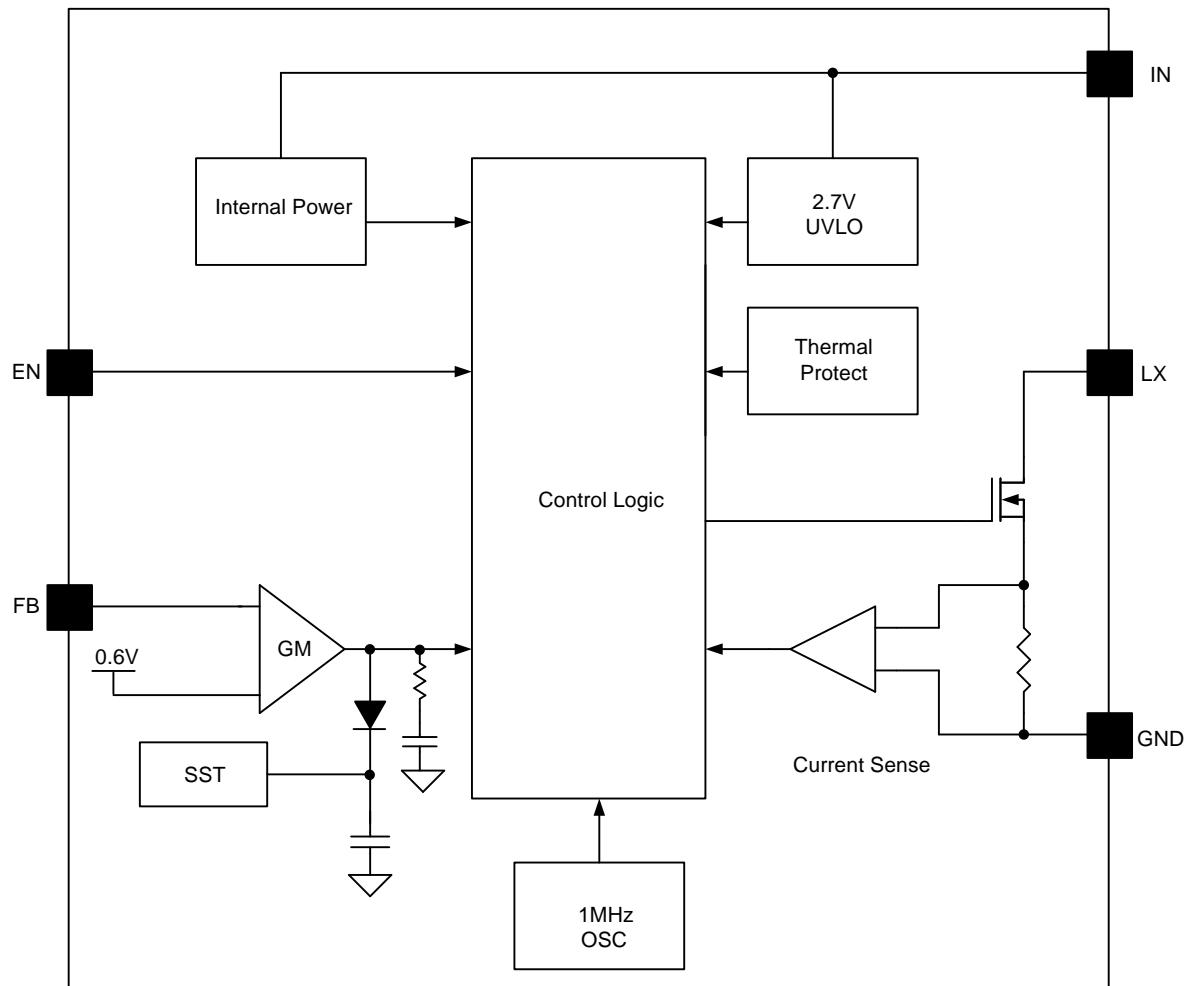
IN ----- 3V to 33V

Junction Temperature Range ----- -40°C to 125°C

Ambient Temperature Range ----- -40°C to 85°C



## Block Diagram





## Electrical Characteristics

(VIN = 5V, VOUT=12V, IOUT=100mA, TA = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V <sub>IN</sub>		3		33	V
Quiescent Current	I <sub>Q</sub>	V <sub>FB</sub> =0.66V		100		µA
Shutdown Current	I <sub>SHDN</sub>	EN=0			15	µA
Low Side Main FET Ron	R <sub>DS(ON)</sub>			120		mΩ
Main FET Current Limit	I <sub>LIM</sub>	Duty cycle=80%	4		6	A
Switching Frequency	F <sub>SW</sub>		0.8	1	1.2	MHz
Feedback Reference Voltage	V <sub>REF</sub>		0.588	0.6	0.612	V
FB Pin Input Current	I <sub>FB</sub>		-50		50	nA
IN UVLO Rising Threshold	V <sub>IN,UVLO</sub>				2.7	V
UVLO Hysteresis	UV <sub>LO,HYS</sub>			0.1		V
EN Rising Threshold	V <sub>ENH</sub>		2			V
EN Falling Threshold	V <sub>ENL</sub>				0.4	V
Max Duty Cycle	D <sub>max</sub>			90		%
Thermal Shutdown Temperature	T <sub>SD</sub>			150		°C
Thermal Recovery Hysteresis	T <sub>HYS</sub>			15		°C

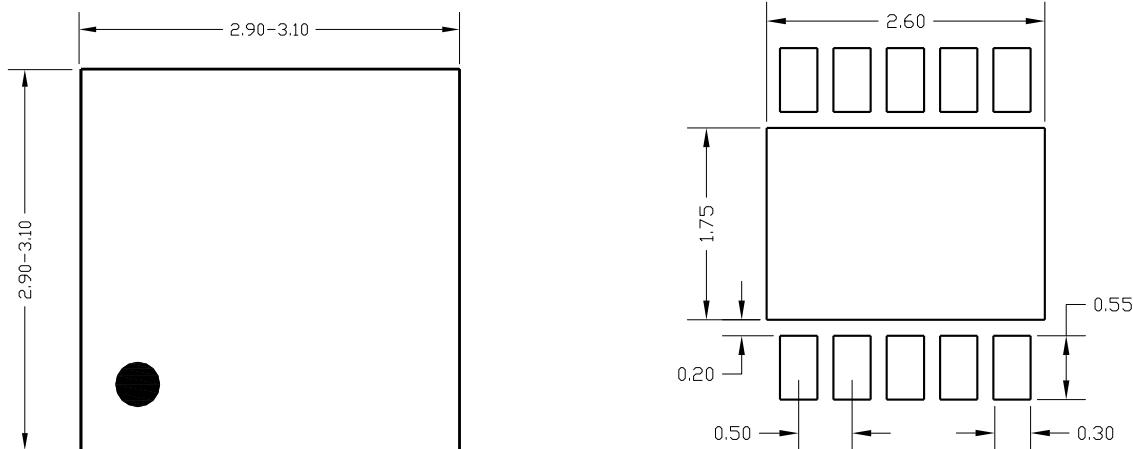
**Note 1:** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2:** θ<sub>JA</sub> is measured in the natural convection at T<sub>A</sub> = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

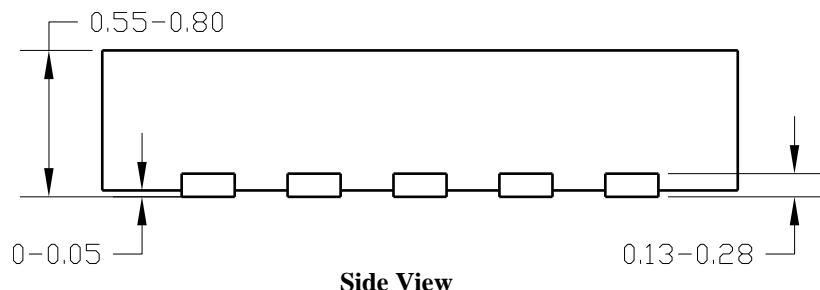


## DFN3x3-10 Package outline

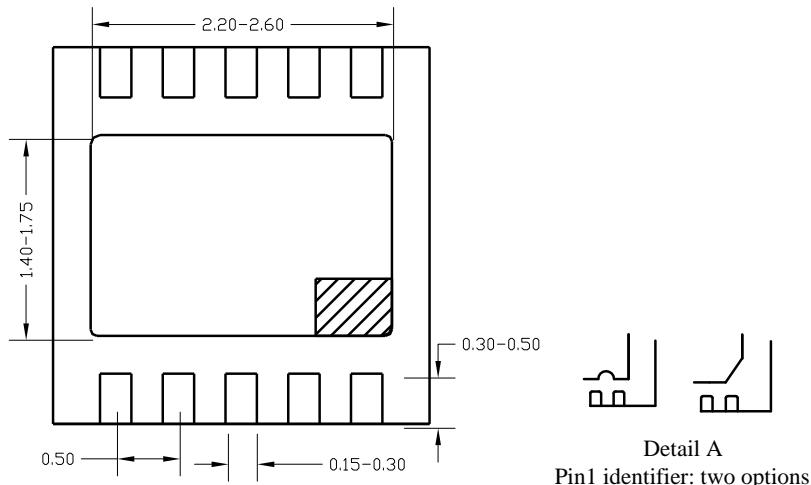


Top View

PCB layout (recommended)



Side View

Detail A  
Pin1 identifier: two options

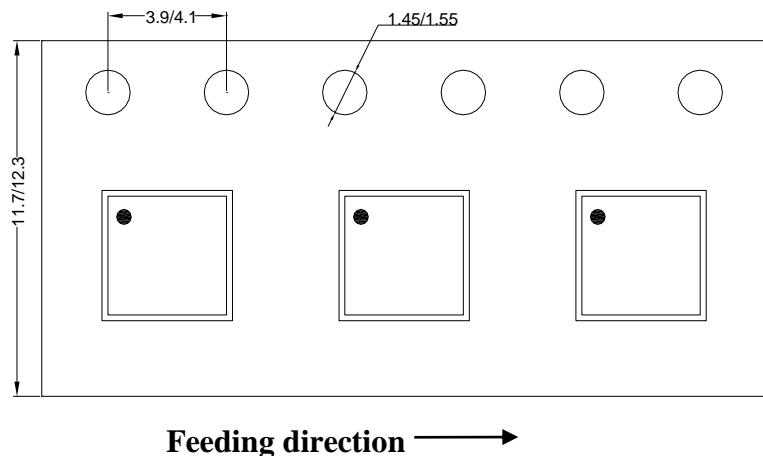
Bottom View

**Notes:** All dimensions are in millimeters and exclude mold flash & metal burr.

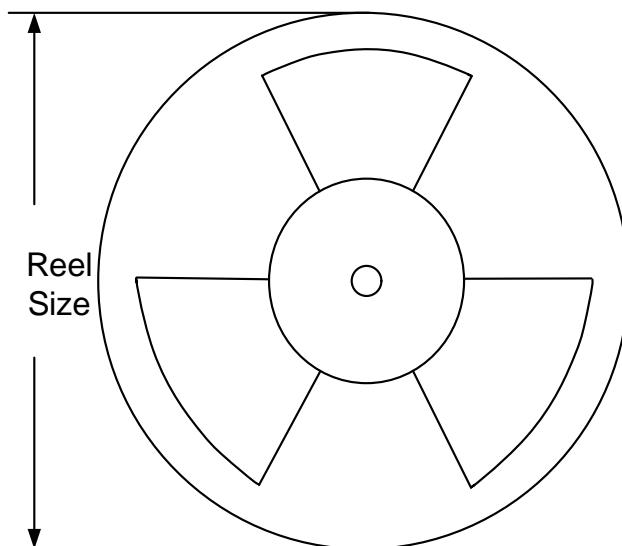
## Taping & Reel Specification



## 1. DFN3x3-10 taping orientation



## 2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3	10	8	13"	400	400	5000

## 3. Others: NA