



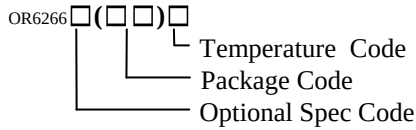
OR6266BQYC

1.8V Minimum Input and 5.5V Maximum Output 6A Peak Current Synchronous Boost with Output Disconnect

General Description

The OR6266/OR6266B is a high efficiency synchronous Boost regulator that converts down to 1.8V input and up to 5.5V output voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch. It can disconnect the output from input during the shutdown mode.

Ordering Information



Ordering Number	Package type	Note
OR6266QYC	QFN2×2-10	----
OR6266BQYC	QFN2×2-10	----

Features

- 1.8V Minimum Input Voltage
- Adjustable Output Voltage from 2.5V to 5.5V
- 6A Peak Current Limit
- Input Under Voltage Lockout
- Load Disconnect during Shutdown
- Output Over Voltage Protection
- Input Battery Voltage Monitor
- Low $R_{DS(ON)}$ (Main Switch/Synchronous Switch) at 5.0V Output: 20/40mΩ
- Automatic Output Discharge at Shutdown:
 - OR6266: Auto Output Discharge Function
 - OR6266BQYC: No Output Discharge Function

Applications

- All Single-cell Li or Dual-cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment.

Typical Applications

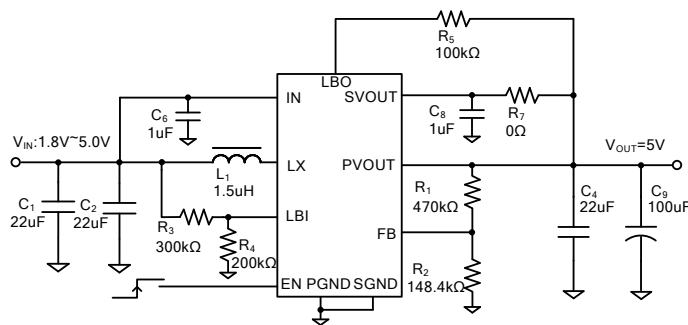


Figure1. Schematic Diagram

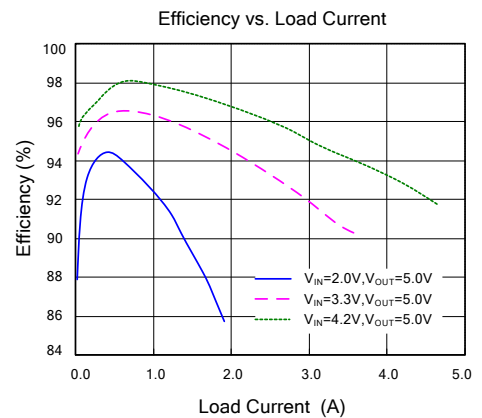
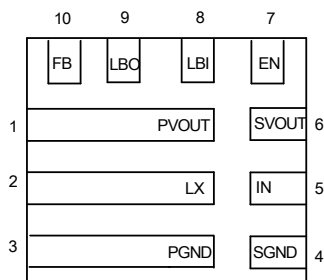


Figure2. Efficiency Figure



Pinout (top view)



(QFN2×2-10)

Top mark: **MGxyz for OR6266BQYC**(Device code: MG, x=year code, y=week code, z= lot number code)

Aaxyz for OR6266BQYC (Device code: Aa, x=year code, y=week code, z= lot number code)

Name	QFN2×2-10	Description
PVOUT	1	Power output pin. Decouple this pin to the GND pin with at least a 22μF ceramic capacitor.
LX	2	Inductor node. Connect an inductor between the IN pin and the LX pin.
PGND	3	Power ground pin.
SGND	4	Signal ground pin.
IN	5	Signal input pin.
SVOUT	6	Signal output pin. Decouple this pin to the GND pin with at least a 1.0μF ceramic capacitor for noise immunity consideration.
EN	7	Enable pin. Internal integrated with a 1MΩ pull-down resistor.
LBI	8	Low battery comparator input.
LBO	9	Low battery comparator output (open-drain).
FB	10	Feedback pin. Connect a resistor R ₁ between the OUT and the FB, and a resistor R ₂ between the FB and the GND to program the output voltage. $V_{OUT}=1.2V\times(R_1/R_2+1)$.

Absolute Maximum Ratings (Note 1)

EN-----V_{OUT}+0.3V

Other Pins----- 6V

Power Dissipation, P_D@ T_A=25°C QFN2×2-10----- 2.5W

Package Thermal Resistance (Note 2)

θ_{JA} ----- 50°C/W

θ_{JC} ----- 10°C/W

Junction Temperature Range ----- 150°C

Lead Temperature (Soldering, 10 sec.) ----- 260°C

Storage Temperature Range ----- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN ----- 1.8V to 5.25V

PVOUT, SVOUT----- 2.5V to 5.5V

EN ----- 0V to V_{OUT}+0.3V

All other pins ----- 0-5.5V

Junction Temperature Range ----- -40°C to 125°C

Ambient Temperature Range ----- -40°C to 85°C



Electrical Characteristics

($V_{IN}=2.4V$, $V_{OUT}=5V$, $I_{OUT}=500mA$, $T_A=25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IN}		1.8		5.25	V
Output Voltage Range	V_{OUT}		2.5		5.5	V
Quiescent Current	V_{IN}	$I_O=0A, V_{EN}=V_{IN}=1.8V$, $V_{OUT}=5.0V$		10		μA
	V_{OUT}			27		μA
Shutdown Current	I_{SHDN}	$V_{EN}=0V, V_{IN}=2.4V$		0.1	1	μA
Linear Charge Current	I_{CHARGE}	$V_{OUT}\leq 1V$		1.2		A
		$1V<V_{OUT}<90\%V_{IN}$		1.0		
Soft-start Time	t_{SS}			1		ms
Input UVLO Threshold	V_{UVLO}				1.78	V
Input UVLO Hysteresis	V_{HYS}			0.1		V
EN Rising Threshold	V_{ENH}		1.2			V
EN Falling Threshold	V_{ENL}				0.4	V
LBI Voltage Threshold	V_{LBI}		1.176	1.2	1.224	V
LBI Input Hysteresis	V_{LBI_HYS}			20		mV
Low Side Main FET R_{ON}	$R_{DS(ON)1}$	$V_{OUT}=5.0V$		20		$m\Omega$
Synchronous FET R_{ON}	$R_{DS(ON)2}$	$V_{OUT}=5.0V$		40		$m\Omega$
Main FET Current Limit	I_{LIM1}		6.0			A
Switching Frequency	f_{SW}			500		kHz
Feedback Reference Voltage	V_{REF}		1.182	1.2	1.218	V
Output Over Voltage Protection	V_{OVP}			6		V
Minimum ON Time	t_{ON_MIN}			100		ns
Minimum OFF Time	t_{OFF_MIN}			100		ns
Max ON Time	t_{ON_MAX}			2		μs
Thermal Shutdown Temperature	T_{SD}			150		$^{\circ}C$
Thermal Shutdown hysteresis	T_{HYS}			20		$^{\circ}C$
Output Discharge Resistor	R_{DSC}			80		Ω

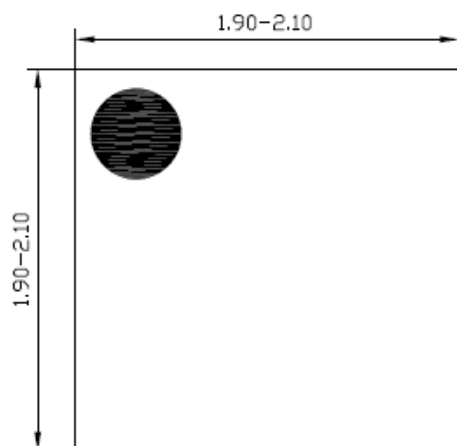
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A=25^{\circ}C$ on a four-layer Orange evaluation board.

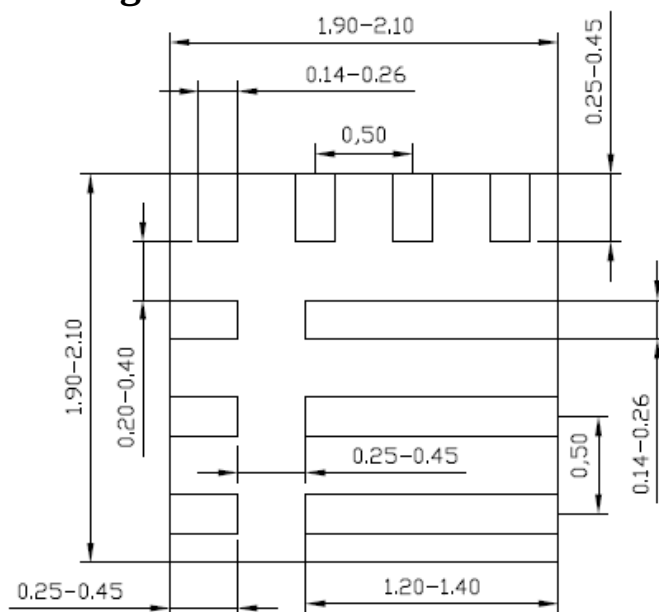
Note 3: The device is not guaranteed to function outside its operating conditions.



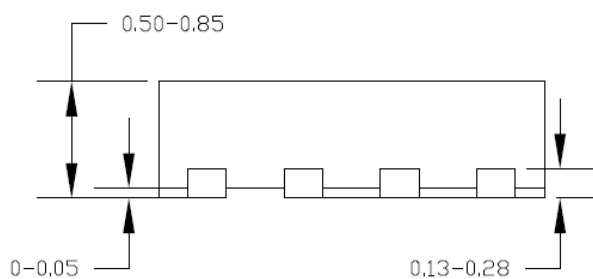
QFN2×2-10 Package Outline



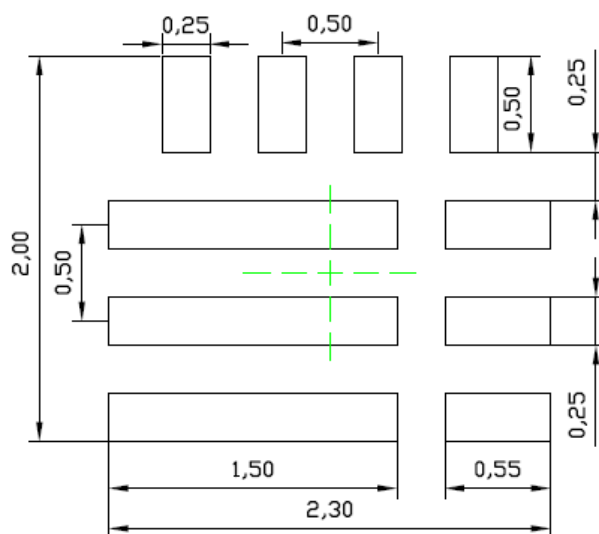
Top View



Bottom View



Side View



**Recommended PCB Layout
(Reference only)**

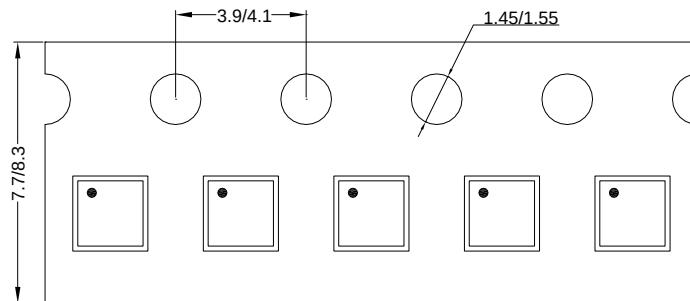
Notes: All dimension in millimeter and exclude mold flash & metal burr.



Taping & Reel Specification

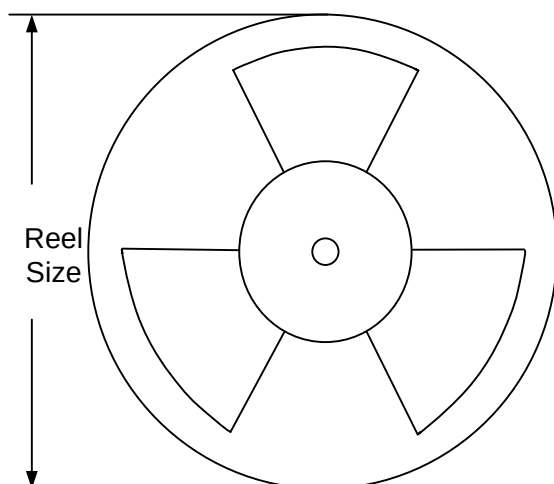
1. Taping orientation

QFN2×2



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2×2	8	4	7"	400	160	3000

3. Others: NA