OR5301BDSC

High Efficiency, 1MHz，1.2A Buck-Boost DC/DC Regulator

General Description

The OR5301BDSC is a wide input voltage range, high efficiency, fixed frequency buck-boost converter that operates from input voltage above, below or equal to the output voltage. It provides a power supply for system powered by either a two-cell or three-cell alkaline, Ni-Cd or Ni-MH battery, or a one -cell Li-Ion or Li -polymer battery.

The OR5301BDSC can support for 1.2A load current capability. It is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. The output voltage and compensation circuit can be programmed using external resistors and capacitors network. During shutdown, the load is disconnected from the battery. The device is packaged in tight DFN3×3-14.

Ordering Information

OR5301□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
OR5301BDSC	DFN3×3-14	----

Features

- Fixed Frequency Operation with Battery Voltage Above, Below or Equal to The Output
- Four Internal Power Switches to Form True 4-Switches Buck-Boost with Single Inductor
- Seamless Buck-Boost Transition
- 2.6V to 5.5V Input Voltage Range
- 1.2A Continuous Output Current Capability
- Output Disconnect at Shutdown
- Power Good Indicator
- Compact Package: DFN3×3-14
- Built In Thermal Shut Down Protection, Hard Short Protection

Applications

- Palmtop Computers
- Handheld Instruments
- MP3/MP4 Players
- Digital Cameras/Camcorders
- Personal Medical Products
- High Power LED's
- All two-cell and three-cell alkaline, Ni-Cd or Ni-MH or signal-cell Li battery powered products

Typical Applications

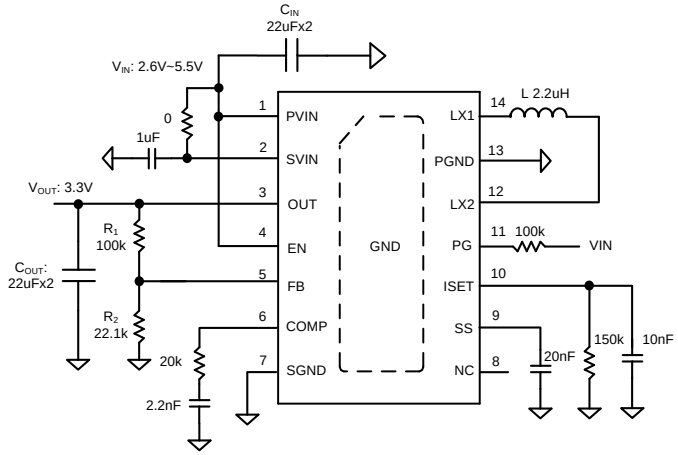


Figure 1. Schematic diagram

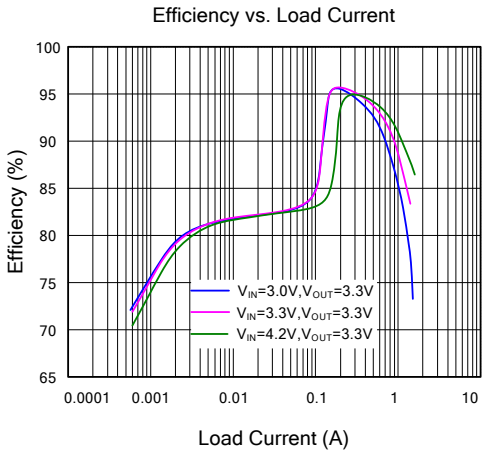
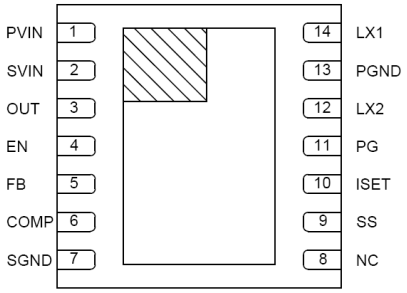


Figure 2. Efficiency Figure

Pinout (top view)



DFN3x3-14

Top Mark: WQ*xyz* (device code: WQ, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Description
PVIN	l	Power input pin. Decouple this pin to GND with at least a 22μF ceramic cap. Minimize the loop area formed by input cap, PVIN pin and GND paddles.
SVIN	2	Signal power input pin. Decouple this pin to GND with at least a 1μF ceramic cap.
OUT	3	Output of the synchronous rectifier. Decouple this pin to GND with at least a 22μF ceramic cap. Minimize the loop area formed by output cap, OUT pin and GND paddles.
EN	4	Enable control. Pull high to turn on. Internal integrated with 1MΩ pull-down resistor.
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage.
COMP	6	External compensation for voltage loop.
SGND	7	Signal ground pin.
NC	8	Not connected.
SS	9	Connect this pin to a soft-start capacitor to program soft-start time.
ISET	10	Apply a resistor and capacitor parallel network to sense the output average current. If V_{ISET} is lower than 0.1V, IC will go into PFM mode. Do not let it floating. Tie to ground for forced PWM operation.
PG	11	Power good indicator.
LX2	12	Inductor connection 2. Connect this node to the switching node of the inductor.
PGND	13	Power ground pin.
LX1	14	Inductor connection 1 Connect this node to the switching node of the inductor.
GND	Paddle	Power ground.

Absolute Maximum Ratings (Note 1)

OUT ---------- 4V
All Other Pins---------- 6V
Power Dissipation, P_D @ T_A = 25°C DFN3×3 ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA} ----------38°C/W
θ_{JC} ---------- 8°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.6V to 5.5V
Output Voltage ---------- 2.6V to 3.8V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 4.2V, V_{OUT} = 3.3V, L =2.2μH, C_{OUT} = 22μF×2, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

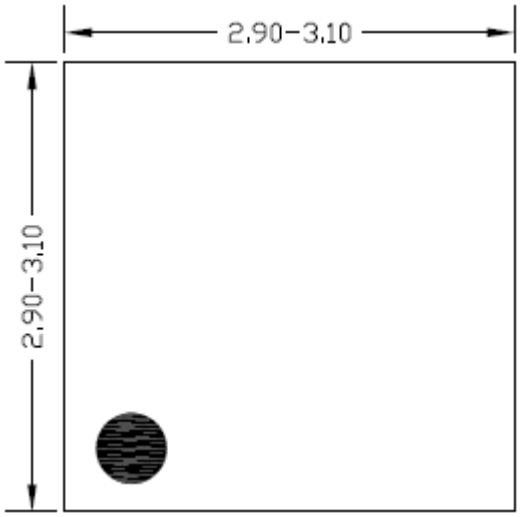
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.6		5.5	V
Output Voltage Range	V_{OUT}		2.6		3.8	V
Quiescent Current	I_Q	I_{OUT}=0, EN=1, ISET=150kΩ, FB=105%×V_{REF}		60	100	μA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
NFET $R_{DS(ON)}$	$R_{DS(ON)1}$			100		mΩ
PFET $R_{DS(ON)}$	$R_{DS(ON)2}$			100		mΩ
Input Peak Current Limit	I_{LIM}		3.5	4		A
Output Negative Current Limit	I_{NEG}			-1		A
Soft-start Current	I_{SS}	Soft-start time: $t_{ss} = \frac{0.7V}{I_{ss}} \times C_{ss}$		5		μA
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Rising Threshold	V_{UVLO}			2.45	2.55	V
UVLO Hysteresis	V_{HYS}			0.2		V
PG Under-voltage Threshold	$V_{FB,UV}$			0.48		V
PG Over-voltage Threshold	$V_{FB,OV}$			0.72		V
Output Current Sense	I_{SET}	I_{OUT}=1A		5		μA
Output Voltage Over Protection	V_{OVP}			125		%
OVP Protection Delay Time	t_{OVP_delay}			16		μs
ISET Pin Threshold for PFM Mode	V_{PFM}		0.08	0.1	0.12	V
Oscillator Frequency	f_{OSC}	I_{OUT}=1.0A	0.8	1.0	1.2	MHz
Min Duty Cycle		Boost & Buck		10		%
Max Duty Cycle		Boost & Buck		90		%
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

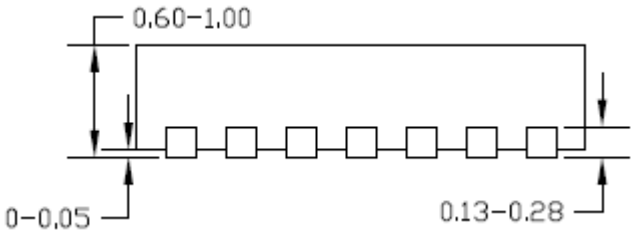
Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of DFN3X3-14 packages is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

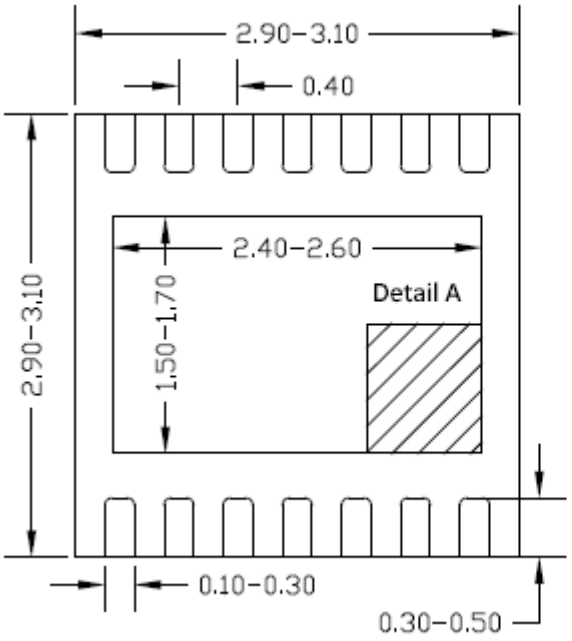
DFN3×3-14 Package Outline Drawing



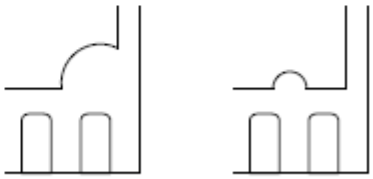
Top View



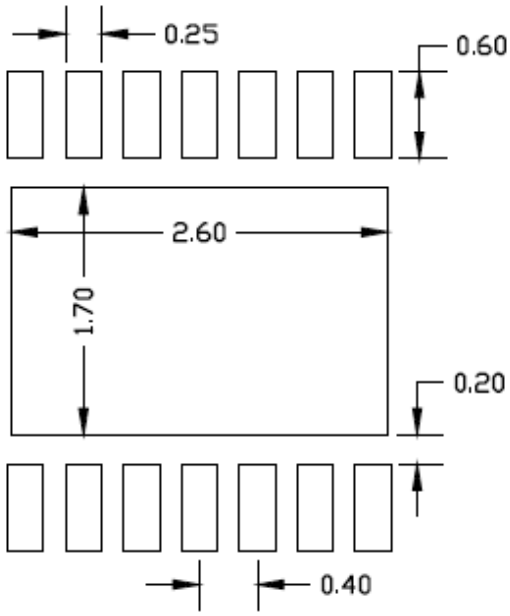
Side View



Bottom View



Detail A
Pin1 Identifier: two options

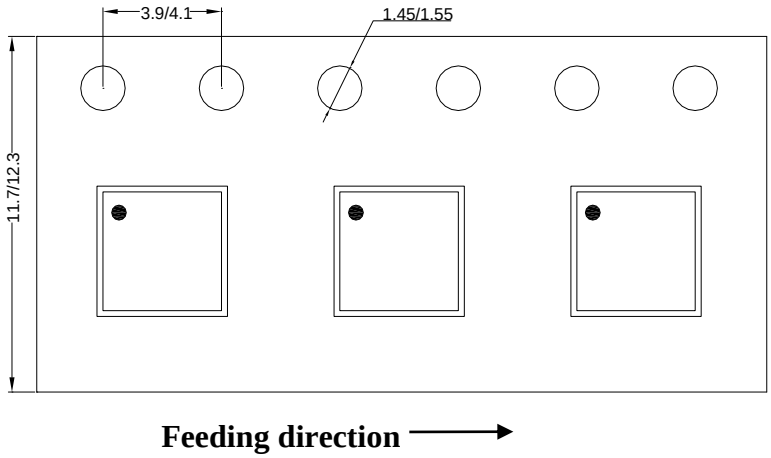


Recommended PCB layout
(Reference only)

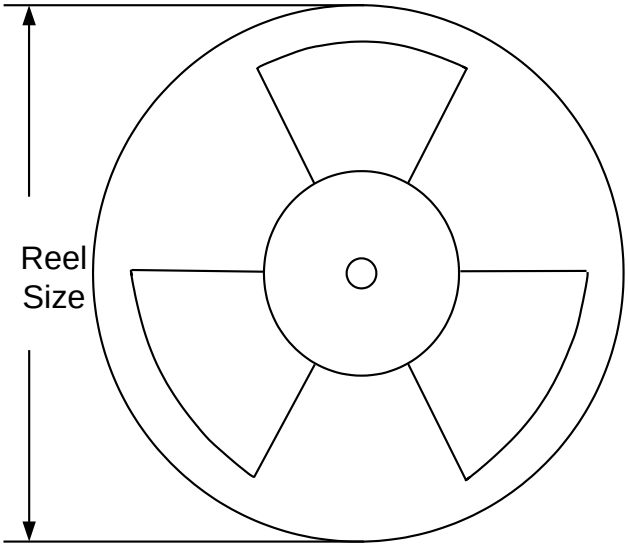
Notes: **All dimension in MM and exclude mold flash & metal burr**

Taping & Reel Specification

1. DFN3×3-14 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3×3	14	8	13"	400	400	5000

3. Others: NA