Application Note: OR1711SDC

High Efficiency, 200kHz, 100V Input, 0.6A Asynchronous Step Down Regulator

General Description

OR1711SDC is a high efficiency, current mode adaptive constant off time controlled asynchronous step-down DC/DC converter capable of delivering 0.6A output current. The OR1711SDC operates over a wide input voltage range from 4.5V to 100V and integrates main switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Ordering Information

OR1711 □(□□)□

└ Temperature Code
Package Code
Optional Spec Code

Ordering Number	Package Type	Note
OR1711SDC	TSOT23-6	

Features

- Low $R_{DS(ON)}$ for Internal N-channel Power FET:1Ω
- 4.5- 100V Input Voltage Range
- 0.6A Output Current Capability
- 200kHz Pseudo Constant Switching Frequency
- Internal Soft-start Limits the Inrush Current
- Hic-cup Mode Output Short Circuit Protection
- EN ON/OFF Control with Accurate Threshold
- Cycle by Cycle Peak Current Limit
- 0.6V±1 % Reference Voltage
- TSOT23-6 Package

Applications

- Non-isolated Telecommunication Buck Regulator
- Secondary High Voltage Post Regulator
- Automotive Systems
- Electric Bicycle

Typical Application

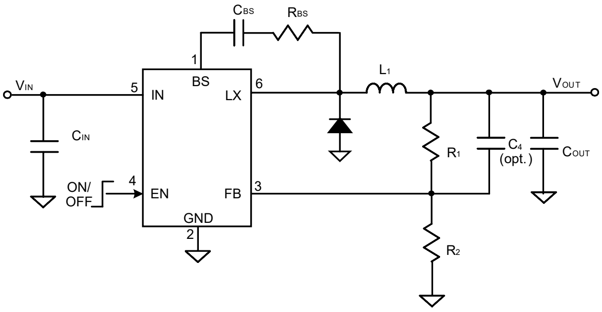


Figure1. Schematic Diagram

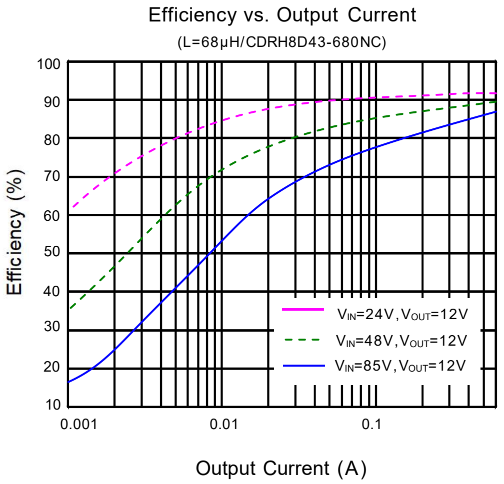
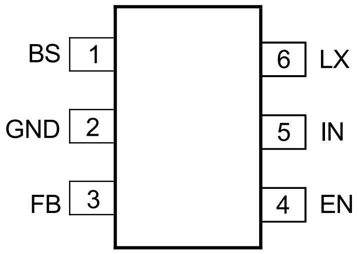


Figure2. Efficiency vs. Output Current

Pinout (top view)



(TSOT23-6)

Top Mark: fK*xyz* (device code: fK, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
BS	1	Boot-strappin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor in series with a10Ω resistor between the BS and the LX pin.
GND	2	Ground pin.
FB	3	Output feedback pin. Connect this pinto the center point of the output resistor divider (as shown in figure 1) to program the output voltage: V_{OUT}=0.6×(1+R1/R2).
EN	4	Enable control. Pull high to turn on. Do not float.
IN	5	Input pin. Decouple this pinto GND pin with at least a 1μF ceramic capacitor.
LX	6	Inductor pin. Connect this pinto the switching node of the inductor.

Function Block

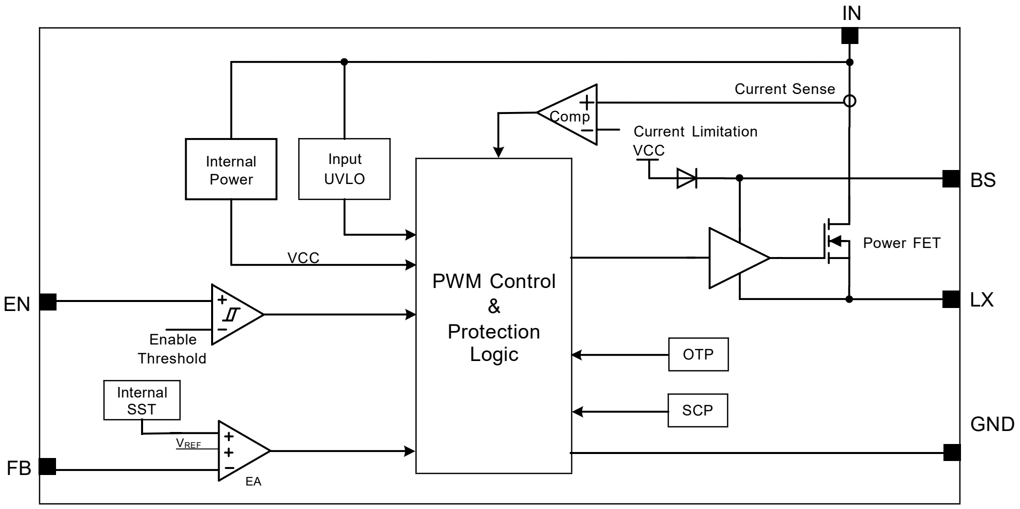


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage --0.3V to 100V
BS-LX Voltage--0.3V to 6V
FB, EN, LX Voltage -- 0.3V to V_{IN} + 0.3V
Power Dissipation, P_D @ T_A = 25°C TSOT23-6 -- 1W
Package Thermal Resistance (Note 2)
θ_{JA} -- 100°C/W
θ_{JC} -- 25°C/W
Junction Temperature Range---40°C to 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range ---65°C to 150°C
Dynamic LX Voltage in10ns Duration-- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage --- 4.5V to 100V
Junction Temperature Range --40°C to 125°C
Ambient Temperature Range --40°C to 85°C

Electrical Characteristics

(V_{IN} = 20V, V_{OUT} = 12V, L = 6.8µH, C_{OUT} = 10µF, T_A = 25°C, I_{OUT} =0.1A, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		100	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		100		µA
Shutdown Current	I_{SHDN}	EN=0		9	20	µA
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
FB Input Current	I_{FB}	V_{FB}=V_{IN}	-50		50	nA
Power FET RON	$R_{DS(ON)1}$			1		Ω
Power FET Peak Current Limit	$I_{LIM,TOP}$		0.9		1.3	A
EN Rising Threshold	V_{ENH}		1.14	1.2	1.26	V
EN Falling Threshold	V_{ENL}		0.94	1	1.06	V
Input UVLO Threshold	V_{UVLO}				4.5	V
Input UVLO Hysteresis	$V_{UVLO, HYS}$			110		mV
Switching Frequency	F_{SW}			200		kHz
Switching Frequency Accuracy	$F_{SW,ACC}$		-20		20	%F_{SW}
Min ON Time	$t_{ON,MIN}$			80		ns
Min Off Time	$t_{OFF,MIN}$			80		ns
Soft-start Time	t_{SS}			800		µs
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

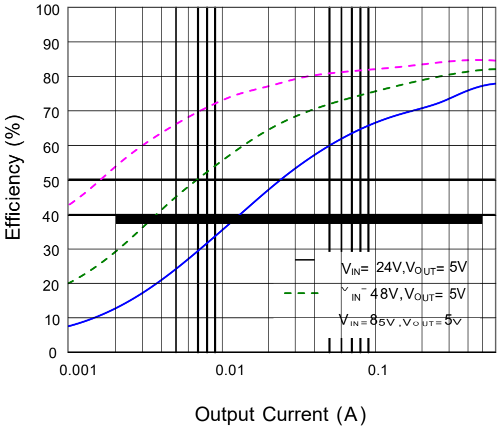
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer orange Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

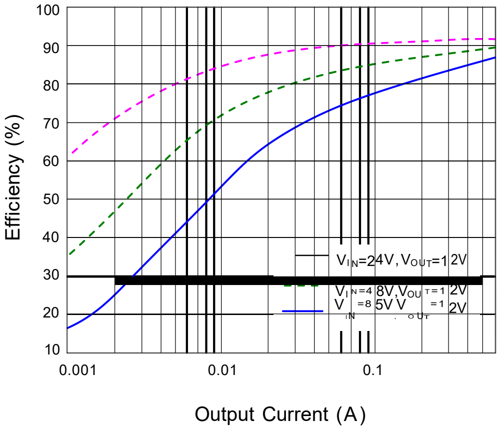
Efficiency vs. Output Current

(L=47µH/CDRH8D43-470NC)



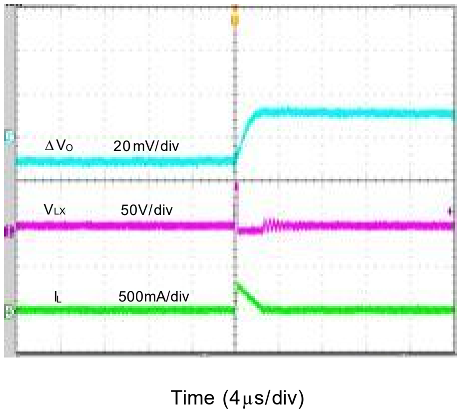
Efficiency vs. Output Current

(L=68µH/CDRH8D43-680NC)



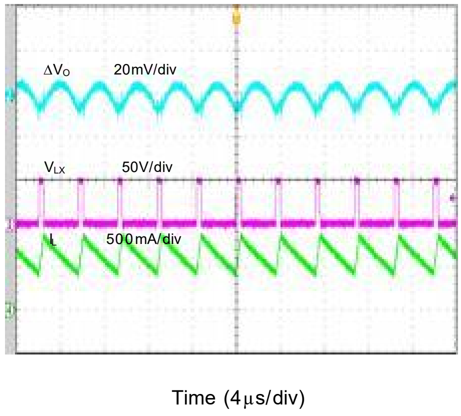
Output Ripple

(V_{IN}=48V, V_{OUT}=5V, I_O=0A)



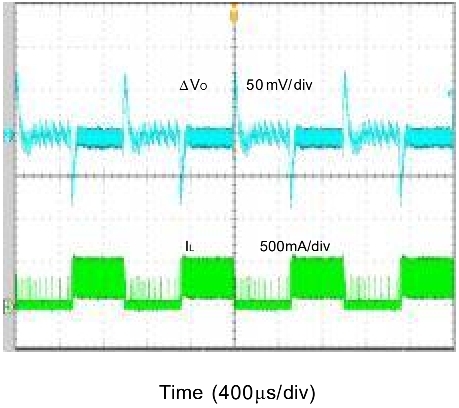
Output Ripple

(V_{IN}=48V, V_{OUT}=5V, I_O=0.6A)



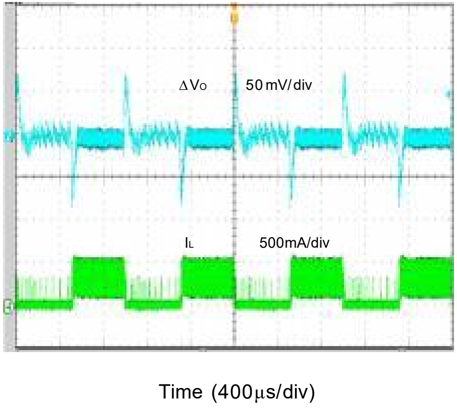
Load Transient

(V_{IN}=48V, V_{OUT}=5V, I_O=0A-0.3A)



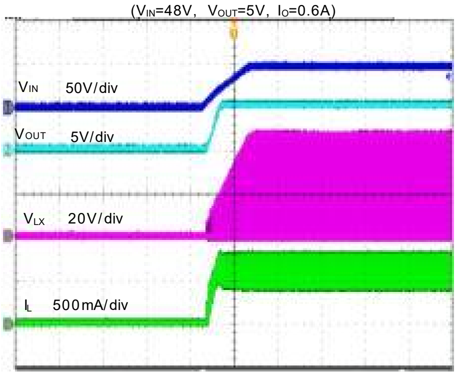
Load Transient

(V_{IN}=48V, V_{OUT}=5V, I_O=0.06A-0.6A)



Startup from V_{IN}

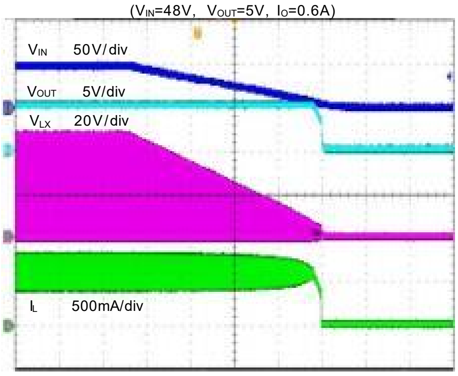
(V_{IN}=48V, V_{OUT}=5V, I_O=0.6A)



Time (4ms/div)

Shutdown from V_{IN}

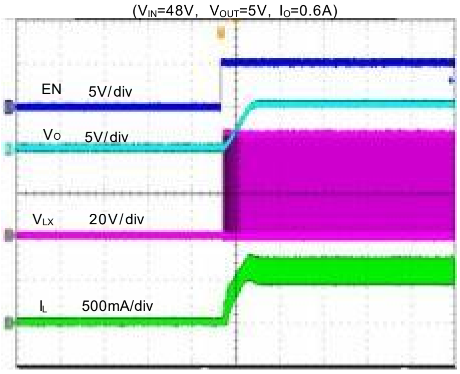
(V_{IN}=48V, V_{OUT}=5V, I_O=0.6A)



Time (10ms/div)

Startup from Enable

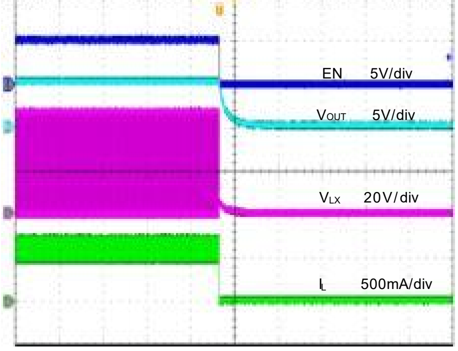
(V_{IN}=48V, V_{OUT}=5V, I_O=0.6A)



Time (2ms/div)

Shutdown from Enable

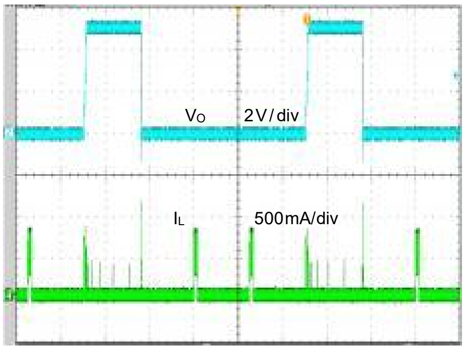
(V_{IN}=48V, V_{OUT}=5V, I_O=0.6A)



Time (2ms/div)

Short Circuit Protection

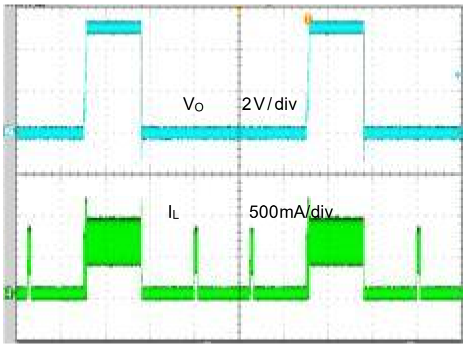
(V_{IN}=48V, V_{OUT}=5V, I_O=0A~Short)



Time (20ms/div)

Short Circuit Protection

(V_{IN}=48V, V_{OUT}=5V, I_O=0.6A~Short)



Time (20ms/div)

Operation

The OR1711SDC is a high efficiency asynchronous step down DC/DC regulator capable of delivering 0.6A output current. The device adopts current mode adaptive constant off time control. The OR1711SDC operates over a wide input voltage range from 4.5V to 100V and integrates main switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Low output voltage ripple and small external inductor and capacitor sizes are achieved at 200kHz switching frequency.

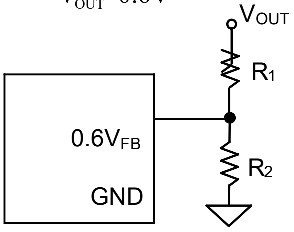
Applications Information

Because of the high integration in the OR1711SDC, the application circuit based on this IC is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L_1 and the feedback resistors (R_1 and R_2) need to be selected for the target applications.

Feedback Resistor Divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 1.2V, R_1=100kΩ is chosen, then using the following equation, R_2 can be calculated to be 100kΩ:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input Capacitor C_{IN}

The ripple current through the input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \text{会} \sqrt{D(1-D)} .$$

To minimize the potential noise problem, we place a typical X5R or a better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} and IN/GND pins. In this case, a 1µF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For most applications, a X5R or a better grade ceramic capacitor larger than 22µF capacitance can work well. The capacitance derating with DC voltage must be considered.

Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \text{会} I_{OUT,MAX} \text{会} 40\%}$$

Where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The OR1711SDC is quite tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \text{会} F_{SW} \text{会} L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

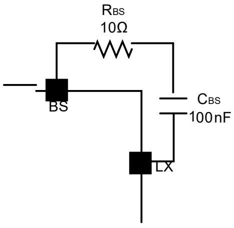
Enable Operation

Pulling the EN pin low (<0.94V) will shut down the device. During the shutdown mode, the OR1711SDC shutdown current will drop to lower than 10µA. Driving the EN pin high (>1.26V) will turn on the IC again.

It is not recommended to connect EN and IN directly. A resistor in a range of 1kohm to 1Mohm should be used if EN is pulled high by IN.

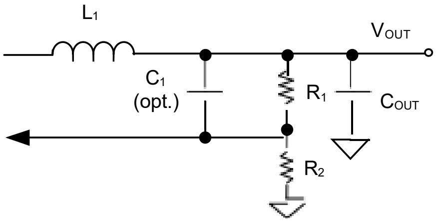
External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor in series with a 10Ω resistor connected between the BS pin and the LX pin is recommended.



Load Transient Considerations

The OR1711SDC integrates the compensation components to achieve good stability and fast transient responses. In some application, adding a 47pF ceramic capacitor in parallel with R_1 may further speed up the load transient responses, thus it is recommended for applications with large load transient step requirements.



Layout Design

The layout design of the OR1711SDC is relatively simple. For the best efficiency and to minimize noise problem, the following components should be placed close to the IC: C_{IN}, L_1, D_1, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connected to the GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane will be highly desirable.

2) C_{IN} must be close to the IN and GND pins. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

4) The components R_1 and R_2 and the trace connected to the FB pin must not be adjacent to the LX node on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at the shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at the shutdown mode.

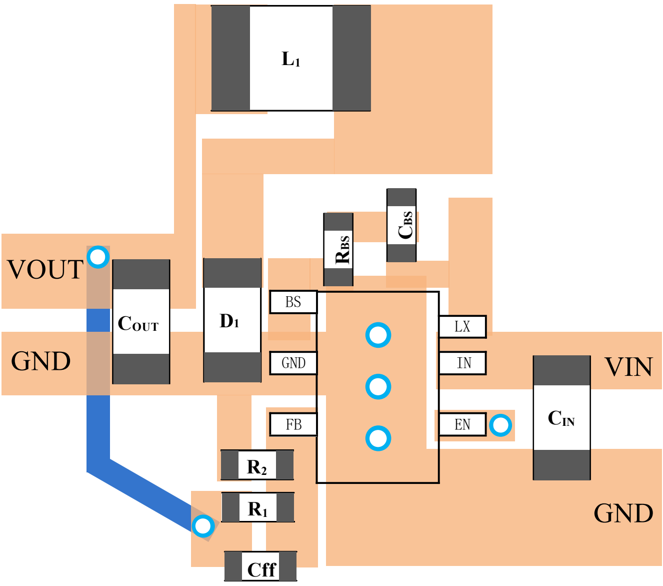
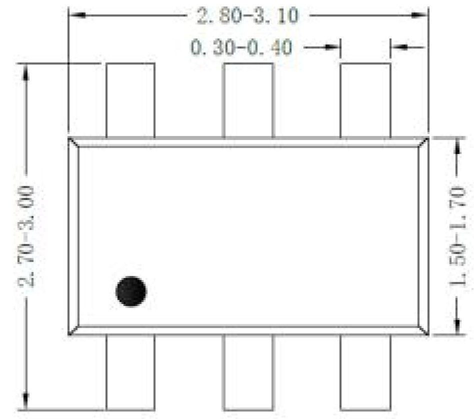
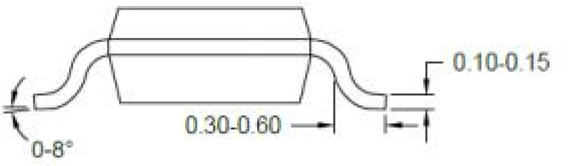


Figure4. PCB Layout Suggestion

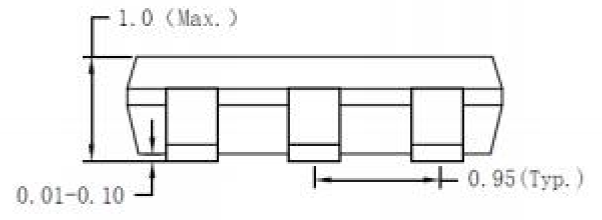
TSOT23-6 Package Outline & PCB Layout



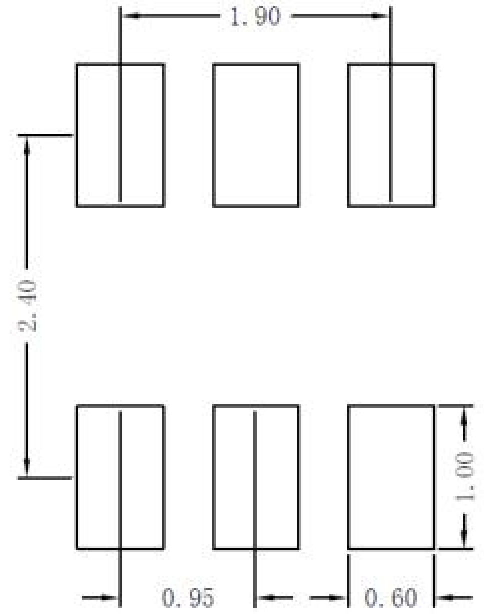
Top view



Side view



Front view



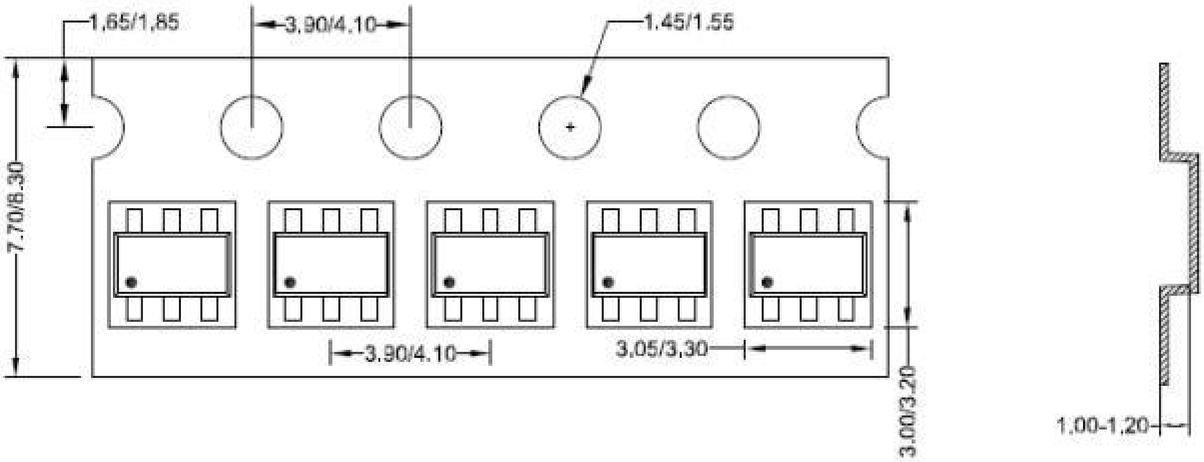
Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

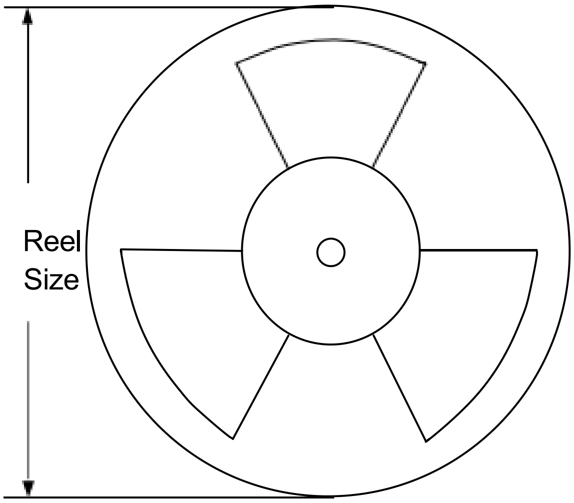
1. Taping orientation

TSOT23-6



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOT23-6	8	4	7"	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jul. 03, 2022	Revision 0.9B	Add a 10Ω resistor in series with the ceramic capacitor between the BS and the LX pin.
Feb. 20, 2019	Revision 0.9A	Max. value of shutdown current changes from 14µA to 20µA in EC table (page3)
Jul. 13, 2018	Revision 0.9	Initial Release

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