OR1627KQKC

High Efficiency 5.5V, 6A, 2.4MHz I²C Programmable, Synchronous Step Down Regulator

General Description

OR1627K is a high efficiency 2.4MHz synchronous stepdown DC/DC regulator IC capable of delivering up to 6A output currents. It can operate over a wide input voltage range from 2.6V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss. The output voltage can be programmed from 0.7125V to 1.5V through I²C interface. OR1627K is in a space saving, low profile CSP1.56x1 .96-20 package.

Features

- Input voltage range: 2.6V to 5.5V
- 2.4 MHz switching frequency minimizes the external components
- Typical 75uA quiescent current
- Low $R_{DS(ON)}$ for internal switches (PFET/NFET): 28mΩ/17mΩ
- Programmable Output Voltage: 0.7125V to 1.5V in 12.5mV steps
- 6A continuous output current capability
- Capable for 0.25uH inductor and 22uF Ceramic Capacitor
- Hic-cup mode protection for hard short condition
- RoHS Compliant and Halogen Free
- Compact package: CSP1.56x1.96-20

Ordering Information

OR1627□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
OR1627KQKC	CSP1.56x1.96-20	0x41H

Applications

- Smart-phone
- Web-tablets

Typical Applications

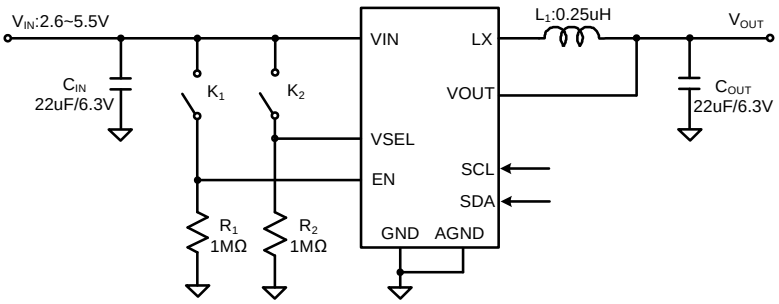


Figure 1. Schematic Diagram

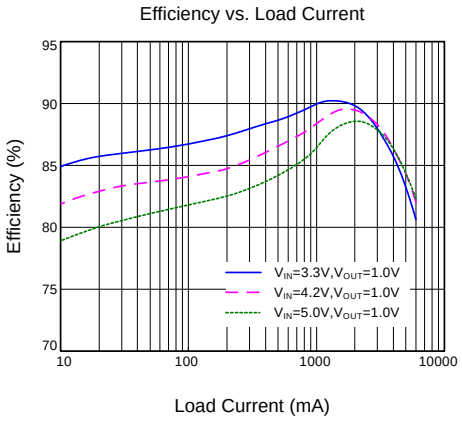
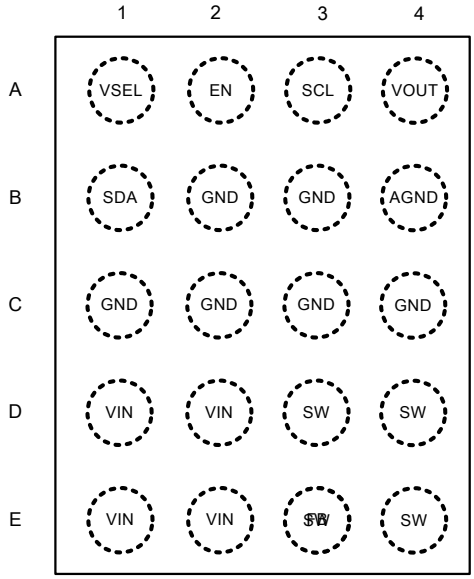


Figure2. Efficiency

Pinout (top view)



Part Number	Package type	Top Mark①
OR1627KQKC	CSP1.56x1.96-20	**Ps**xyz

Note①： ***x=year code, y=week code, z= lot number code.***

Pin	Pin Name	Pin Description
D1,D2,E1,E2	VIN	Power input pin. These pins must be decoupled to ground with at least 22uF ceramic capacitor. The input capacitor should be placed as close as possible between VIN and GND pins.
D3,D4,E3,E4	SW	Switching node pin. Connect these pins to the switching node of inductor.
B2,B3,C1,C2,C3,C4	GND	Power ground pins.
A1	VSEL	Voltage select pin. When this pin is low, V_{OUT} is set by the VSEL0 register. When this pin is high, V_{OUT} is set by the VSEL1 register.
A2	EN	Enable control pin. Active high. Do not leave it floating.
B1	SDA	I^2C interface Bi-directional Data line.
B4	AGND	Analog ground pin.
A3	SCL	I^2C interface clock line.
A4	VOUT	Sense pin for output. Connect to the output capacitor side.

Absolute Maximum Ratings (Note 1)

VIN---------- 6.0V
All Other Pins---------- V_{IN} + 0.6V
Power Dissipation, P_D @ T_A = 25℃ CSP1.56x1.96-20---------- 2.6W
Package Thermal Resistance (Note 2)
θ_{JA} ----------38℃/W
θ_{JC} ---------- 8℃/W
Junction Temperature Range ---------- 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.6V to 5.5V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.0V, L = 0.25uH, C_{OUT} = 22uF, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.6		5.5	V
V_{IN} UVLO	V_{UVLO}	V_{IN} Rising		2.45	2.60	V
V_{IN} UVLO Hysteresis	V_{UVHYST}			150		mV
Quiescent Current	I_Q	I_{OUT}=0, EN=1, FB=105%*V_{REF}		75		μA
Shutdown Current	$I_{SHDN\_H/W}$	EN=0		0.1		μA
	$I_{SHDN\_S/W}$	EN=V_{IN}, Buck_ENx=0		30		
EN, VSEL, SDA, SCL						
Rising threshold	V_{IH}		1.1			V
Falling threshold	V_{IL}				0.4	V
V_{OUT} Accuracy	V_{REG}	Forced PWM, V_{OUT}=VSEL0, default value	-1.5		+1.5	%
NFET $R_{DS(ON)}$	$R_{DS(ON)N}$			17		mΩ
PFET $R_{DS(ON)}$	$R_{DS(ON)P}$			28		mΩ
PMOS peak current limit	I_{LIM_PEAK}		7.5			A
NMOS peak current limit	I_{LIM_VALLEY}		6			A
Internal soft-start time	t_{SS}			300		us
Min on time				40		ns
Oscillator Frequency	F_{OSC}			2.4		MHz
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃
LX node discharge resistor	R_{DSH}			150		Ω
Input OVP shutdown	V_{OVP}	Rising threshold		6.15		V
		Falling threshold	5.5	5.85		V
Over voltage protection blanking time	$T_{Blanking}$			20		us

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Enabling Function

The EN pin controls OR1627KQKCstart up. EN pin low to high transition starts the power up sequence. If EN pin is low, the DC/DC converter will be turned off.
OR1627Kallows software to enable of the regulator when EN is HIGH, via the BUCK_EN bits. BUCK_EN0 and BUCK_EN1 are both initialized HIGH in the registers.

Hardware and Software Enable control table.

Pins		Bits		
EN	VSEL	BUCK_EN0	BUCK_EN1	OUTPUT
0	x	x	x	OFF
1	0	0	x	OFF
1	0	1	x	ON
1	1	x	0	OFF
1	1	x	1	ON

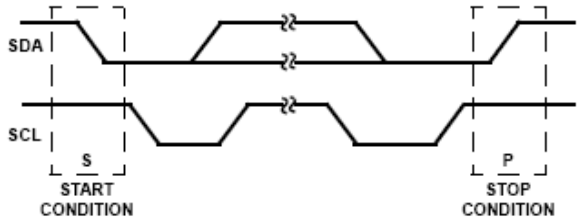
Input Over Voltage Protection Function

When the V_{IN} exceeds over voltage protection threshold, OR1627K will stop switching to protect the circuitry. An internal 20us blanking time helps to prevent the circuit from shutting down due to noise spikes.

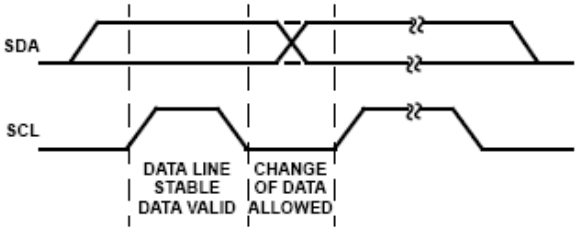
I²C Interface

OR1627Kfeatures an I²C interface that allow the HOST processor to control the output voltage achieve the DVS function. The I²C interface supports clock speeds of up to 3.4MHz and uses standard I²C commands. OR1627K always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation. I²C address of the OR1627Kis set at the factory to 0x41h.

START and STOP Conditions:
OR1627Kis controlled via an I²C compatible interface. The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.

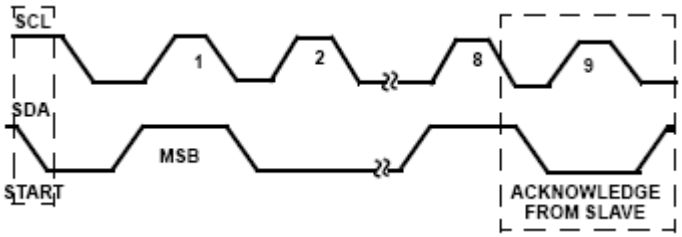


Data Validity:
The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



Acknowledge:

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

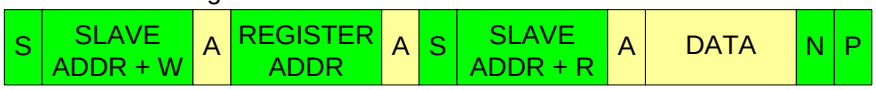


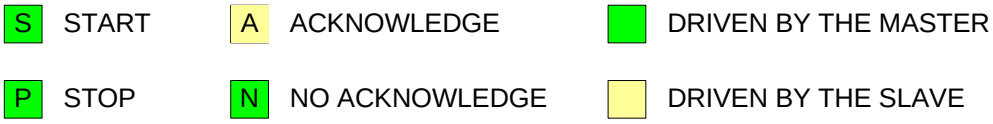
Data Transactions:

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address (1000001x for the OR1627K, this address can be changed if necessary) followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and OR1627Kacknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the O R 1 6 2 7 K which register the master will write or read. Once the OR1627Kreceives a register address byte it responds with an acknowledge.

Write To A Register

Read From A Register





Register Settings:

1. VSEL0 (0x00)

Register Name				VSEL0
Address				0x00
Field	**Bit**	**R/W**	**Default**	**Description**
BUCK_EN0	7	R/W	1	Software buck enable. When EN pin is low, the regulator is off. When EN pin is high, BUCK_EN bit takes precedent.
MODE0	6	R/W	0	0=Allow auto-PFM mode during light load. 1=Forced PWM mode
NSEL0	5:0	R/W	010111 (V_{OUT}=1.0V)	000000 = 0.7125V 000001 = 0.7250V 000010 = 0.7375V …… 010111 = 1.0000V …… 111111 =1.5000V

2. VSEL1 (0x01)

Register Name				VSEL1
Address				0x01
Field	**Bit**	**R/W**	**Default**	**Description**
BUCK_EN1	7	R/W	1	Software buck enable. When EN pin is low, the regulator is off. When EN pin is high, BUCK_EN bit takes precedent.
MODE1	6	R/W	0	0=Allow auto-PFM mode during light load. 1=Forced PWM mode
NSEL1	5:0	R/W	010111 (V_{OUT}=1.0V)	000000 = 0.7125V 000001 = 0.7250V 000010 = 0.7375V …… 010111 = 1.0000V …… 111111 =1.5000V

3. Control Register (0x02)

Register Name				Control Register
Address				0x02
Field	**Bit**	**R/W**	**Default**	**Description**
Output Discharge	7	R/W	1	0 = discharge resistor is disabled. 1 = discharge resistor is enabled.
Slew Rate	6:4	R/W	000=12.5mV/0.15us	Set the slew rate for positive voltage transitions. 000 = 12.5mV/0.15us 001 = 12.5mV/0.3us 010 = 12.5mV/0.6us 011 = 12.5mV/1.2us 100 = 12.5mV/2.4us 101 = 12.5mV/4.8us 110 = 12.5mV/9.6us 111 = 12.5mV/19.2us
Reserved	3	R/W	0	Always reads back 0.
RESET	2	R/W	0	Setting to 1 resets all registers to default values.
Reserved	1:0	R/W	00	Always reads back 0.

4. ID1 Register (0x03)

Register Name				ID1 Register
Address				0x03
Field	**Bit**	**R/W**	**Default**	**Description**
VENDOR	7:5	R	100	IC vendor Orange code.
Reserved	4	R	0	Always reads back 0.
DIE_ID	3:0	R	1000	IC option code

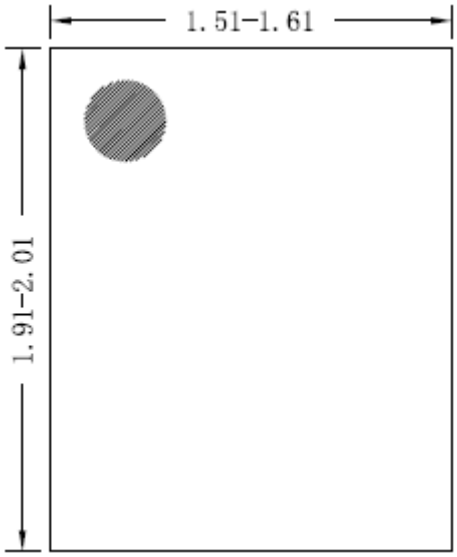
5. ID2 Register (0x04)

Register Name				ID2 Register
Address				0x04
Field	**Bit**	**R/W**	**Default**	**Description**
Reverved	7:4	R	0000	Always reads back 0.
DIE_REV	3:0	R	0001	IC mask revision code

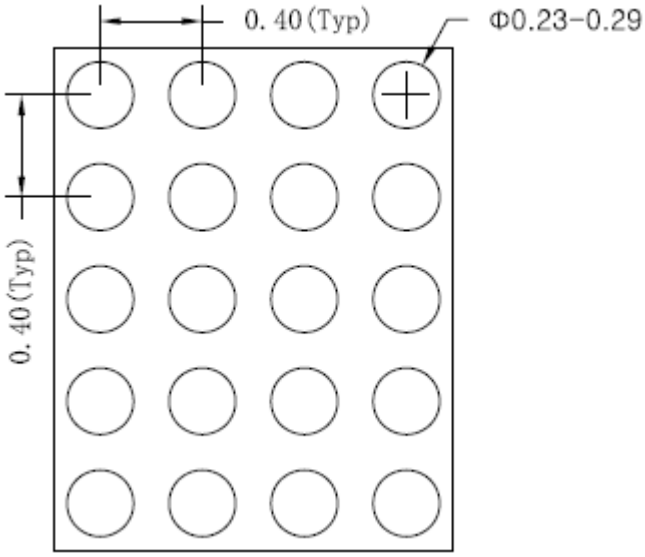
6. PGOOD Register (0x05)

Register Name				PGOOD Register
Address				0x05
Field	**Bit**	**R/W**	**Default**	**Description**
PGOOD	7	R	0	1: Buck is enabled and soft-start is completed.
Reserved	6:0	R	000 0000	Always reads back 0.

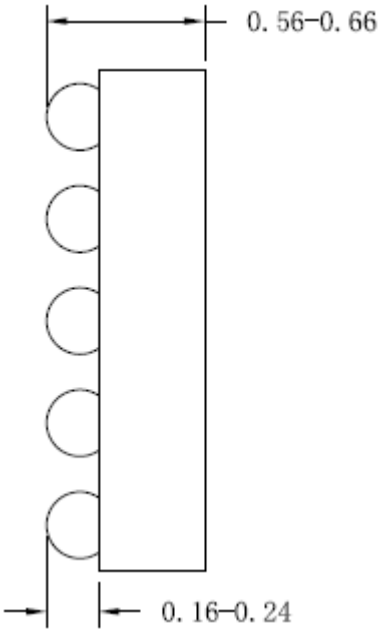
CSP1.56×1.96-20 Outline Drawing



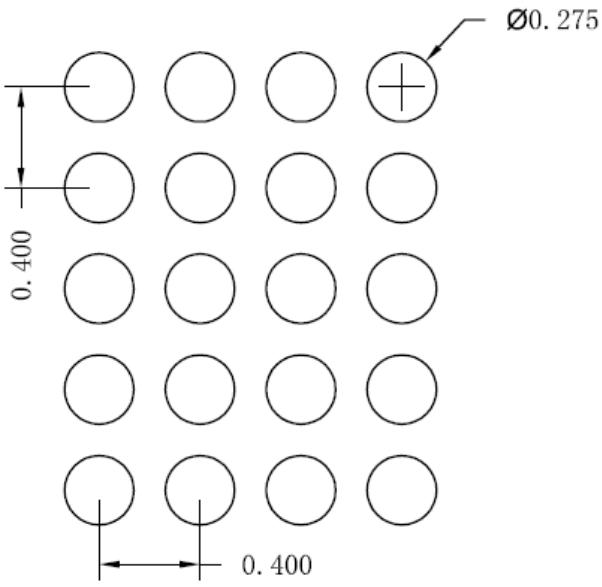
Top View



Bottom View



Side View

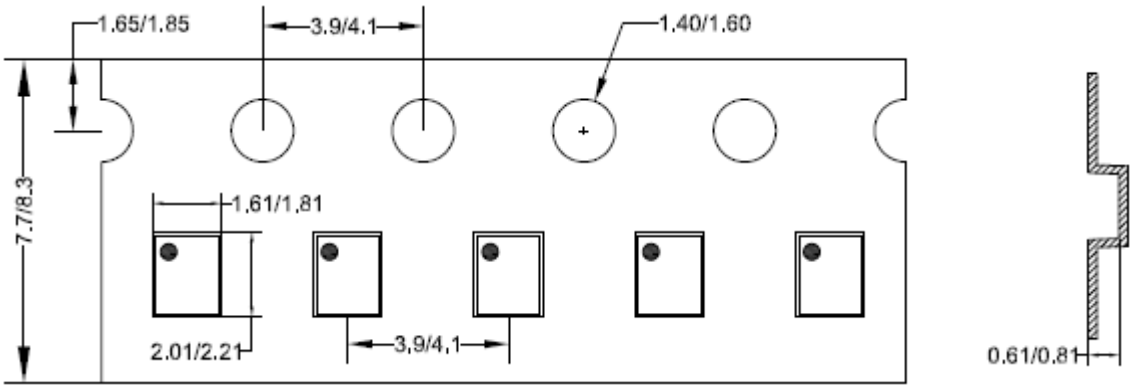


Recommended PCB Layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

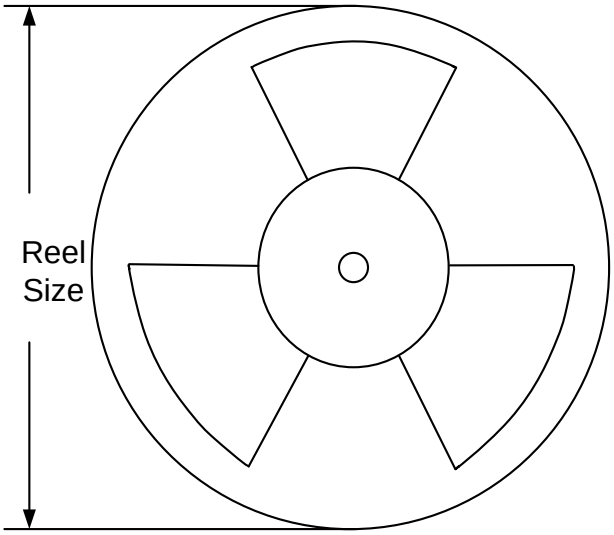
Taping & Reel Specification

1. CSP1.56×1.96



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
CSP1.56×1.96	8	4	7"	400	400	3000

3. Others: NA