



OR1588THC

High Efficiency Fast Response, 8A, 28V Input Synchronous Step Down Regulator

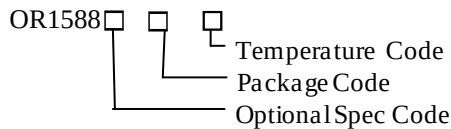
General Description

The OR1588THC develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 8A current over a wide input voltage range of 4.5V to 24V.

Oranges proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

Internal 30mΩ power and 15mΩ synchronous rectifier switches provide excellent efficiency over a range of applications, especially for low output voltages and low duty cycles. The OR1588 also integrates a bypass switch which allows the IC to be powered by external DC source. Cycle-by-cycle current limit, input under voltage lock-out, internal soft-start, output under voltage protection and over voltage protection and thermal shutdown provide safe operation in all operating conditions. The OR1588THC is available in a compact QFN2.5×2.5-16 package.

Ordering Information



Ordering Number	Package type	Note
OR1588THC	QFN2.5×2.5-16	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 30/15mΩ
- Wide Input Voltage Range: 4.5~24V
- Integrated Bypass Switch: 1.2Ω
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- Pseudo-Constant Frequency: 500kHz
- Adjustable Output Voltage Application
- 8A Output Current Capability
- $\pm 1\%$ Internal Reference Voltage
- PFM/USM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Discharge Function
- Cycle-by-cycle Valley and Peak Current Limit Protection
- Programmable Valley Current Limit Threshold by ILMT Pin
- Latch-off Mode Output Under Voltage Protection
- Latch-off Mode Output Over Voltage Protection
- Latch-off Mode Over Temperature Protection
- Input UVLO
- RoHS Compliant and Halogen Free
- Compact Package: QFN2.5×2.5-16

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

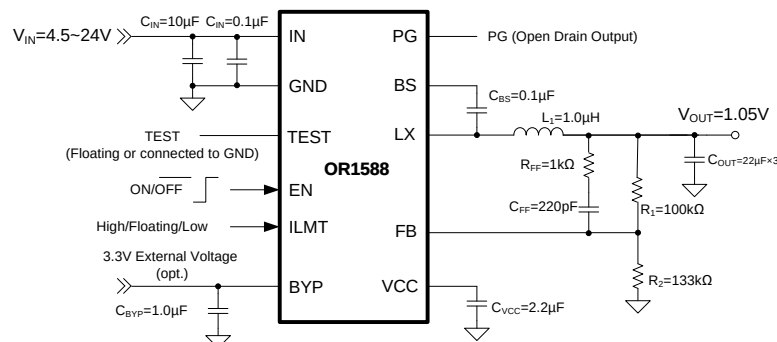


Figure1. Schematic Diagram

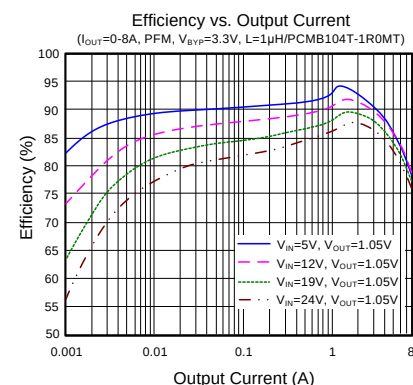
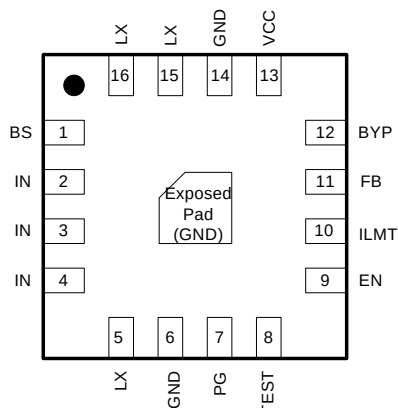


Figure2. Efficiency vs. Output Current



Pinout (top view)



(QFN2.5×2.5-16)

Top Mark: Kdxyz (Device code: Kd, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
IN	2, 3, 4	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor. A 0.1μF input ceramic capacitor is recommended to reduce the input noise.
LX	5, 15, 16	Inductor pin. Connect this pin to the switching node of the inductor.
GND	6, 14, EP	Ground pin.
PG	7	Power good Indicator. Open-drain output when the output voltage is within 90% to 120% of the regulation point.
TEST	8	For factory use only. Leave this pin floating or connect it to GND in application.
EN	9	Enable control of the DC/DC regulator. Pulling this pin high to turn on the regulator. Do not leave this pin floating. The pin is also used for controlling operation mode of the regulator under light load condition after the output of Buck regulator is within the regulation range. When its voltage is less than 1.6V, the Buck regulator works under ultra-sonic mode. When its voltage is larger than 2.2V, the Buck regulator works under PFM mode.
ILMT	10	Valley current limit threshold selection pin.
FB	11	Output feedback pin. Connected to the center point of the resistor divider.
BYP	12	External 3.3V bypass power supply input. Decouple this pin to the GND with a 1μF ceramic capacitor. Leave this pin floating if it is not used.
VCC	13	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to the GND with a 2.2μF ceramic capacitor. This pin cannot support external supply.



Block Diagram

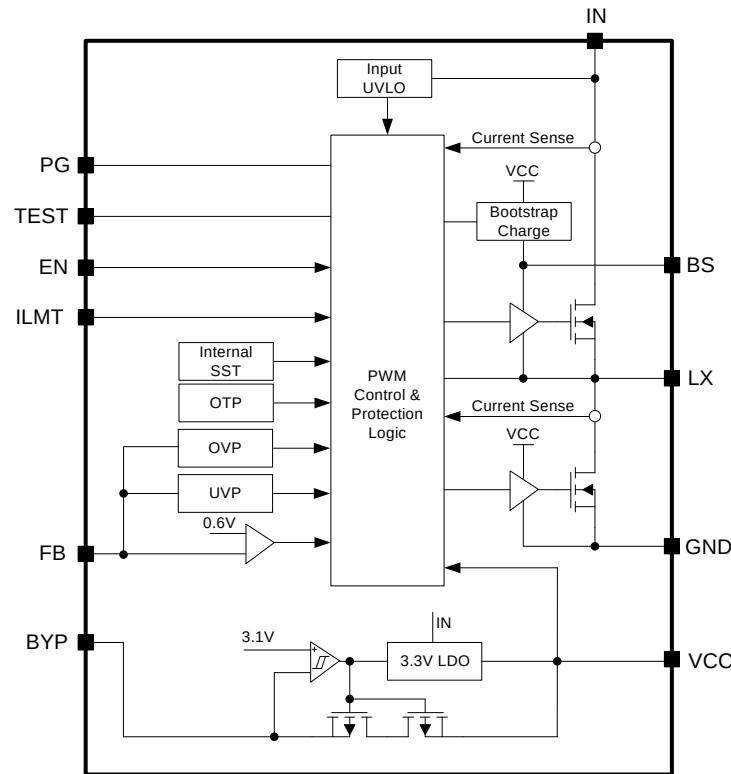


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage	-----	-0.3V to 28V
IN-LX, LX, PG, TEST, EN Voltage	-----	-0.3V to 26V
BS-LX, FB, VCC, ILMT Voltage	-----	-0.3V to 4V
BYP Voltage	-----	-0.3V to 6V
Maximum Power Dissipation, $P_{D,MAX}$, @ $T_A = 25^{\circ}C$ QFN2.5×2.5-16	-----	3W
Package Thermal Resistance (Note 2)		
θ_{JA} , QFN2.5×2.5-16	-----	33°C/W
θ_{JC} , QFN2.5×2.5-16	-----	5.5°C/W
Junction Temperature Range	-----	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Storage Temperature Range	-----	-65°C to 150°C
Dynamic LX Voltage in 10ns Duration	-----	-5V to 29V
Dynamic LX Voltage in 20ns Duration	-----	-1V to 28V

Recommended Operating Conditions (Note 3)

Supply Input Voltage	-----	4.5V to 24V
Junction Temperature Range	-----	-40°C to 125°C
Ambient Temperature Range	-----	-40°C to 85°C



Electrical Characteristics

($V_{IN}=12V$, $C_{OUT}=100\mu F$, $T_A=25^{\circ}C$, $I_{OUT}=1A$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		24	V
Input UVLO Threshold	V_{UVLO}	V_{IN} rising			4.2	V
UVLO Hysteresis	V_{HYS}			0.3		V
Quiescent Current	I_Q	$I_{OUT}=0A$, $V_{OUT}=V_{SET} \times 105\%$		100	130	μA
Shutdown Current	I_{SHDN}	EN=0		5	9	μA
Feedback Reference Voltage	V_{REF}		0.594	0.600	0.606	V
FB Input Current	I_{FB}	$V_{FB}=1V$	-50		50	nA
Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			30		m Ω
Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			15		m Ω
Output Discharge Current	I_{DIS}	$V_{OUT}=1.2V$		40		mA
Top FET Current Limit	$I_{LMT, TOP}$		15	17.5	20	A
Bottom FET Current Limit	$I_{LMT, BOT}$	ILMT=Low	8			A
		ILMT=Floating	10			A
		ILMT=High	12			A
Bottom FET Reverse Current Limit	$I_{LMT, RVS}$	USM mode		3		A
Soft-start Time	tss	V_{OUT} from 0% to 100% V_{SET} (Note 4)		600		μs
EN Input Voltage High	$V_{EN, H}$		1			V
EN Input Voltage Low	$V_{EN, L}$				0.4	V
EN Voltage for Ultra-sonic Mode	$V_{EN, USM}$		1		1.6	V
EN Voltage for PFM Mode	$V_{EN, PFM}$		2.2		V_{IN}	V
Internal EN Resistor to GND	R_{EN}			2.5		M Ω
ILMT Input Voltage High	$V_{ILMT, H}$		$V_{CC}-0.8$			V
ILMT Input Voltage Low	$V_{ILMT, L}$				0.4	V
Switching Frequency	f _{SW}	$V_{OUT}=1.2V$, CCM	410	500	590	kHz
Ultra-sonic Mode Frequency	f _{USM}	USM mode, $I_{OUT}=0A$		27		kHz
Min ON Time	t _{ON, MIN}	$V_{IN}=V_{IN, MAX}$ (Note 4)		50		ns
Min OFF Time	t _{OFF, MIN}			200		ns
VCC Output Voltage	V_{CC}	VCC adds 1mA load		3.37		V
Output Over Voltage Threshold	V_{OVP}	V_{FB} rising	117	120	123	% V_{REF}
Output Over Voltage Hysteresis	$V_{OVP, HYS}$			5		% V_{REF}
Output OVP Delay	t _{OVP, DLY}	(Note 4)		20		μs
Output Under Voltage Protection Threshold	V_{UVP}		55	60	65	% V_{REF}
Output UVP Delay	t _{UVP, DLY}	(Note 4)		200		μs
Power Good Rising Threshold	$V_{PG, R}$	V_{FB} rising (good)	86	90	94	% V_{REF}
Power Good Falling Threshold	$V_{PG, F}$	V_{FB} falling	81	85	89	% V_{REF}
Power Good Delay	t _{PG, R}	Low to high (Note 4)		200		μs
	t _{PG, F}	High to low (Note 4)		10		μs
Power Good Low Voltage	$V_{PG, LOW}$	$V_{FB}=0V$, $I_{PG}=5mA$			0.4	V
Bypass Switch $R_{DS(ON)}$	$R_{DS(ON), BYP}$			1.2		Ω
Bypass Switch Turn-on Voltage	V_{BYP}		2.75	3.1		V
Bypass Switch Switchover Hysteresis	$V_{BYP, HYS}$			0.2		V
Bypass Switch OVP Threshold	$V_{BYP, OVP}$			120		% V_{CC}
Thermal Shutdown Temperature	T _{OTP}	T _J rising (Note 4)		150		$^{\circ}C$
Thermal Shutdown Hysteresis	T _{OTP, HYS}	(Note 4)		15		$^{\circ}C$



Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

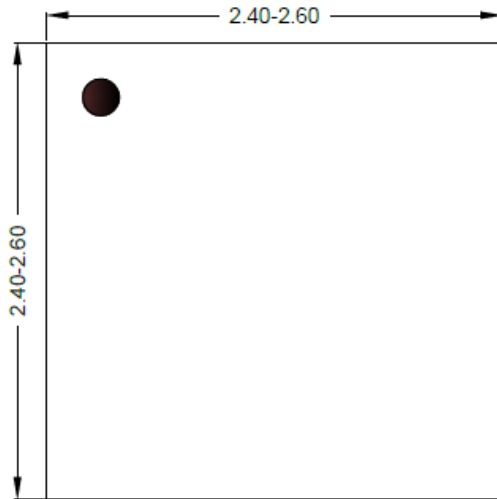
Note 2: Package thermal resistance is measured in the natural convection at $T_A = 25^{\circ}\text{C}$ on a 8.5cm×8.5cm size, four-layer Orange Evaluation Board with 2-oz copper.

Note 3: The device is not guaranteed to function outside its operating conditions.

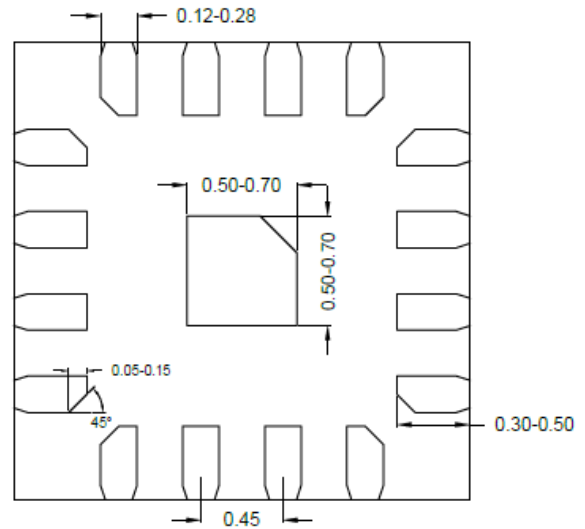
Note 4: Guaranteed by design.



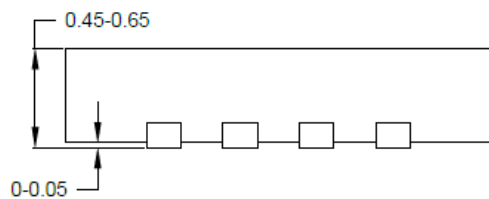
QFN2.5×2.5-16 Package Outline Drawing



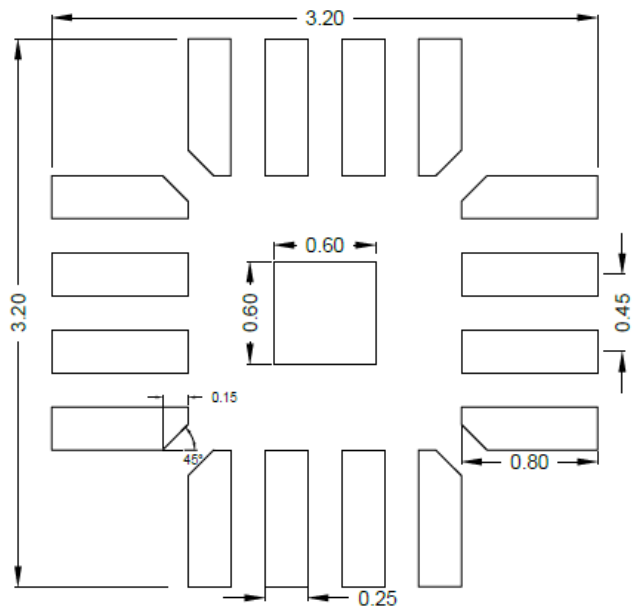
Top view



Bottom view



Side view



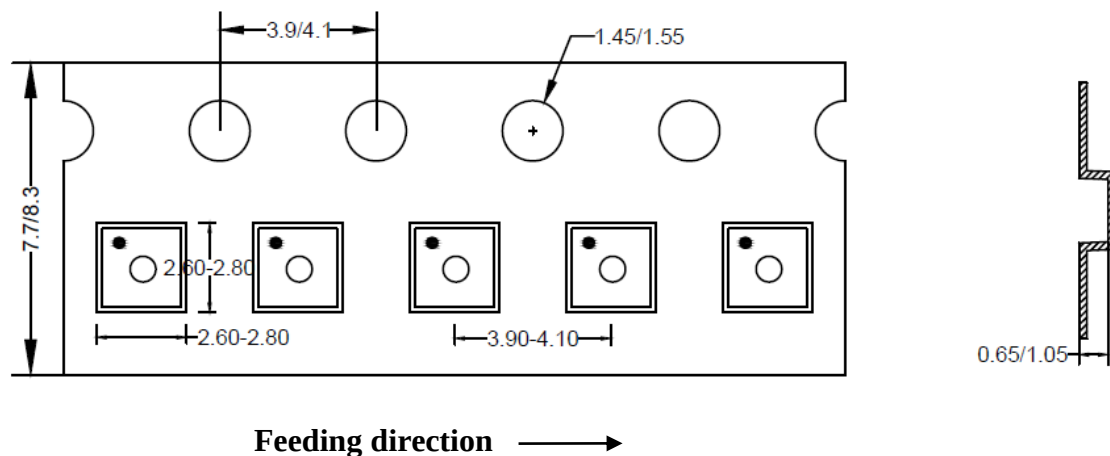
Recommended PCB layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

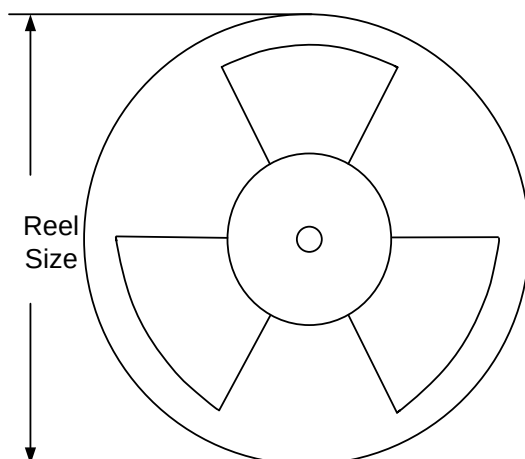


Taping & Reel Specification

1. QFN2.5×2.5 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2.5×2.5	8	4	7"	400	160	3000

3. Others: NA