OR1570BYC

High Efficiency Fast Response, 11A, 28V Input Synchronous Step Down Regulator

General Description

The OR1570BYC develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 11A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss . In addition, it operates at pseudo-constant frequency of 500kHz under heavy load conditions to minimize the size of inductor and capacitor.

Orange's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

The OR1570BYC operates over a wide input voltage range from 4V to 24V. Cycle-by-cycle current limit, input under voltage lock-out, internal soft-start, output under voltage protection, over voltage protection and thermal shutdown provide safe operation in all operating conditions.

Ordering Information

OR1570□ □ □
- □: Temperature Code
- □: Package Code
- □: Optional Spec Code

Ordering Number	Package type	Note
OR1570BYC	QFN3×4-13	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 17/7.5 mΩ
- Wide Input Voltage Range: 4~24V
- Integrated Bypass Switch: 1.5Ω
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- Pseudo-Constant Frequency: 500kHz
- Adjustable Output Voltage Application
- 11A Output Current Capability
- ±1% Internal Reference Voltage
- PFM/USM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Discharge Function
- Cycle-by-cycle Valley and Peak Current Limit Protection
- Programmable Valley Current Limit Threshold by ILMT Pin
- Latch-off Mode Output Under Voltage Protection
- Latch-off Mode Output Over Voltage Protection
- Latch-off Mode Over Temperature Protection
- Input UVLO
- RoHS Compliant and Halogen Free
- Compact Package: QFN3×4-13

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP
- Desk-top

Typical Applications

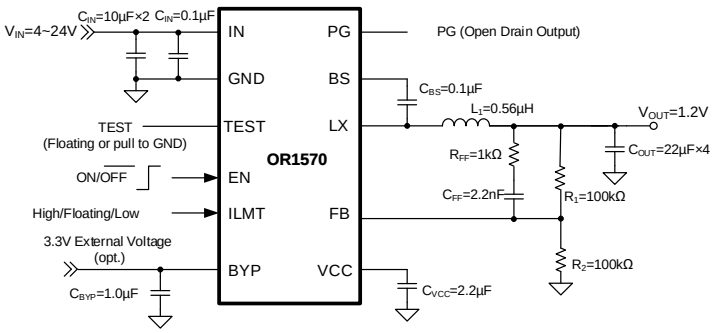


Figure1. Schematic Diagram

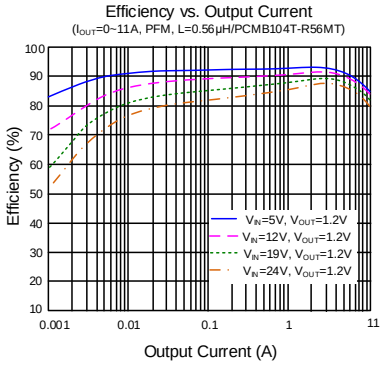
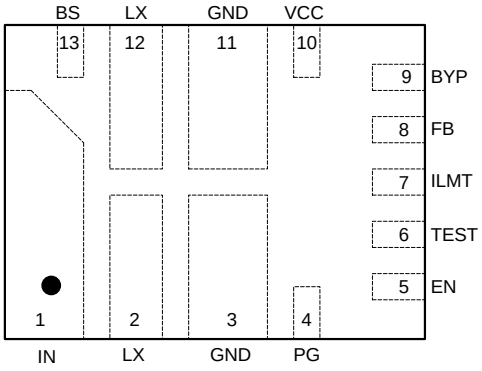


Figure2. Efficiency vs. Output Current

Pinout (top view)



(QFN3×4-13)

Top Mark: **CUR*xyz*** (Device code: CUR, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
IN	1	Input pin. Decouple this pin to the GND pin with at least a 20µF ceramic capacitor. A 0.1µF input ceramic capacitor is recommended to reduce the input noise.
LX	2, 12	Inductor pin. Connect this pin to the switching node of the inductor.
GND	3, 11	Ground pin.
PG	4	Power good Indicator. Open drain output when the output voltage is within 90% to 120% of the regulation point.
EN	5	Enable control of the DC/DC regulator. Pull this pin high to turn on the regulator. Do not leave this pin floating. The pin is also used for controlling operation mode of the regulator under light load condition after the output of buck regulator is within the regulation range. When its voltage is less than 1.6V, the Buck regulator works under ultra-sonic mode. When its voltage is larger than 2.2V, the Buck regulator works under PFM mode.
TEST	6	For factory use only. Leave this pin floating or connect it to the GND in application.
ILMT	7	Valley current limit threshold selection pin.
FB	8	Output feedback pin. Connect to the center point of the resistor divider.
BYP	9	External 3.3V bypass power supply input. Decouple this pin to GND with a 1µF ceramic capacitor. Leave this pin floating or connect it to GND if not used.
VCC	10	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. This pin cannot support external power supply. Decouple this pin to GND with a 2.2µF ceramic capacitor.
BS	13	Boot-strap pin. Supply high side gate driver. Connect a 0.1µF ceramic capacitor between the BS pin and the LX pin.

Block Diagram

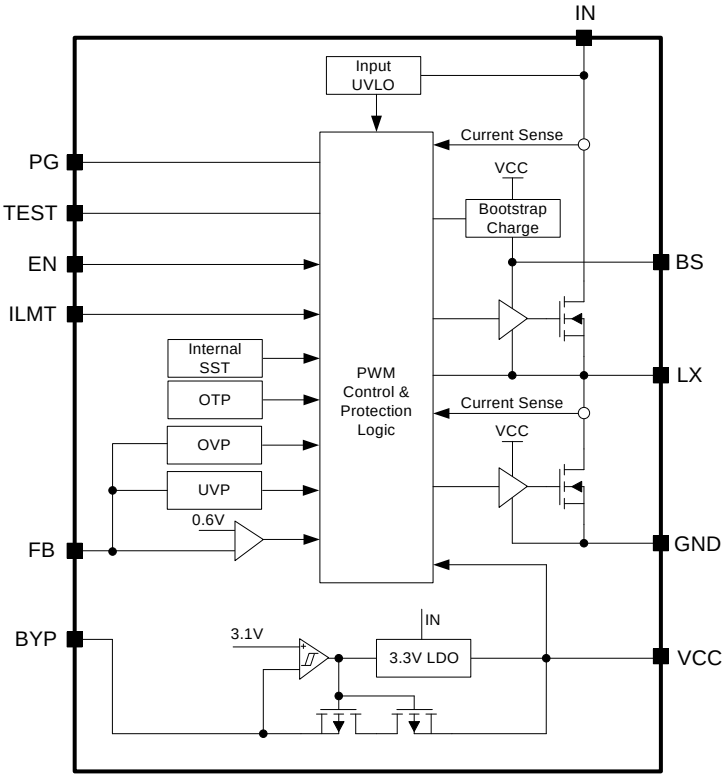


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 28V
IN-LX, LX, PG, TEST, EN Voltage---------- -0.3V to 26V
BS-LX, FB, VCC, BYP, ILMT Voltage---------- -0.3V to 4V
Maximum Power Dissipation, $P_{D,MAX,}$ @ T_A = 25°C QFN3×4-13 ---------- 3.7W
Package Thermal Resistance (Note 2)
θ_{JA}, QFN3×4-13 ---------- 27°C/W
θ_{JC}, QFN3×4-13 ---------- 4.3°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX Voltage in 10ns Duration ---------- -5V to 29V
Dynamic LX Voltage in 20ns Duration ---------- -1V to 28V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 24V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN}= 12V, C_{OUT}= 100µF, T_A= 25°C, I_{OUT}= 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		24	V
Input UVLO Threshold	V_{UVLO}	V_{IN} rising			3.9	V
UVLO Hysteresis	V_{HYS}			0.5		V
Quiescent Current	I_Q	I_{OUT}=0A, V_{BYP}=0V, V_{OUT}=V_{SET}×105%		140		µA
Shutdown Current	I_{SHDN}	EN=0		4	9	µA
Feedback Reference Voltage	V_{REF}		0.594	0.600	0.606	V
FB Input Current	I_{FB}	V_{FB}=1V	-50		50	nA
Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			17		mΩ
Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			7.5		mΩ
Output Discharge Current	I_{DIS}	V_{OUT}=1.2V		40		mA
Top FET Current Limit	$I_{LMT,TOP}$			24		A
Bottom FET Current Limit	$I_{LMT,BOT}$	ILMT=Low	12.5			A
		ILMT=Floating	15			A
		ILMT=High	18			A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$	USM Mode	4	6		A
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100%V_{SET}		600		µs
EN Input Voltage High	$V_{EN,H}$		1			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
EN Voltage for Ultra-sonic Mode	$V_{EN,USM}$		1		1.6	V
EN Voltage for PFM Mode	$V_{EN,PFM}$		2.2		V_{IN}	V
ILMT Input Voltage High	$V_{ILMT,H}$		2.5			V
ILMT Input Voltage Low	$V_{ILMT,L}$				0.5	V
Switching Frequency	f_{SW}	V_{OUT}=1.2V, CCM	425	500	575	kHz
Ultra-sonic Mode Frequency	f_{USM}	USM mode, I_{OUT}=0A		27		kHz
Min ON Time	$t_{ON,MIN}$	V_{IN}=$V_{IN,MAX}$		50		ns
Min OFF Time	$t_{OFF,MIN}$			200		ns
VCC Output Voltage	V_{CC}	VCC adds 1mA load	3.1	3.3	3.5	V
Output Over Voltage Threshold	V_{OVP}	V_{FB} rising	117	120	123	%V_{REF}
Output Over Voltage Hysteresis	$V_{OVP,HYS}$			5		%V_{REF}
Output OVP Delay	$t_{OVP,DLY}$	(Note 4)		30		µs
Output Under Voltage Protection Threshold	V_{UVP}		55	60	65	%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$	(Note 4)		200		µs
Power Good Threshold	V_{PG}	V_{FB} falling(not good)	80	83	86	%V_{REF}
Power Good Hysteresis	$V_{PG,HYS}$	V_{FB} rising (good)		7		%V_{REF}
Power Good Delay	$t_{PG,R}$	Low to high (Note 4)		200		µs
	$t_{PG,F}$	High to low (Note 4)		20		µs
Power Good Low Voltage	$V_{PG,LOW}$	V_{FB}=0V, I_{PG}=5mA			0.45	V
Bypass Switch $R_{DS(ON)}$	$R_{DS(ON),BYP}$			1.5		Ω
Bypass Switch Turn-on Voltage	V_{BYP}		2.97	3.1		V
Bypass Switch Switchover Hysteresis	$V_{BYP,HYS}$			0.2		V
Bypass Switch OVP Threshold	$V_{BYP,OVP}$			120		%V_{LDO}
Thermal Shutdown Temperature	T_{OTP}	T_J rising (Note 4)		150		°C
Thermal Shutdown Hysteresis	$T_{OTP,HYS}$	(Note 4)		15		°C

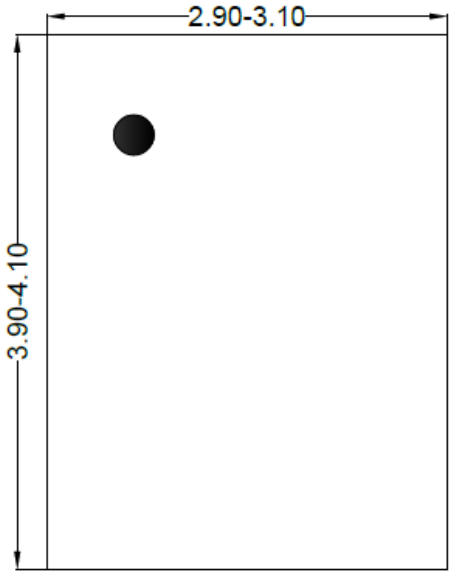
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a 8.5cm×8.5cm size, four-layer OrangeEvaluation Board with 2-oz copper.

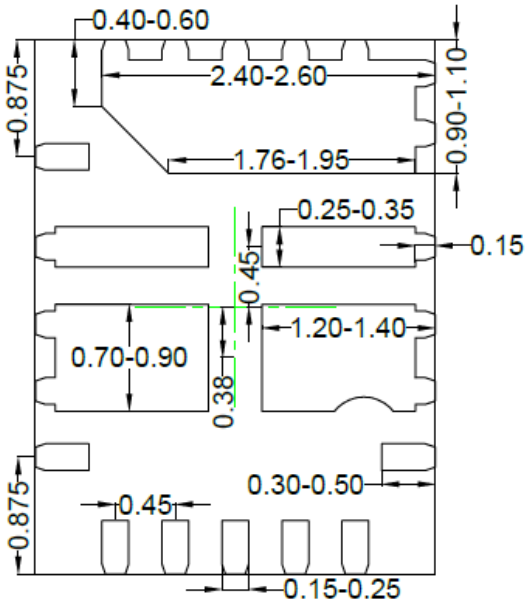
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

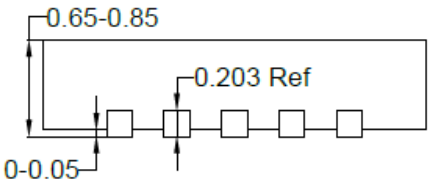
QFN3×4-13 Package Outline Drawing



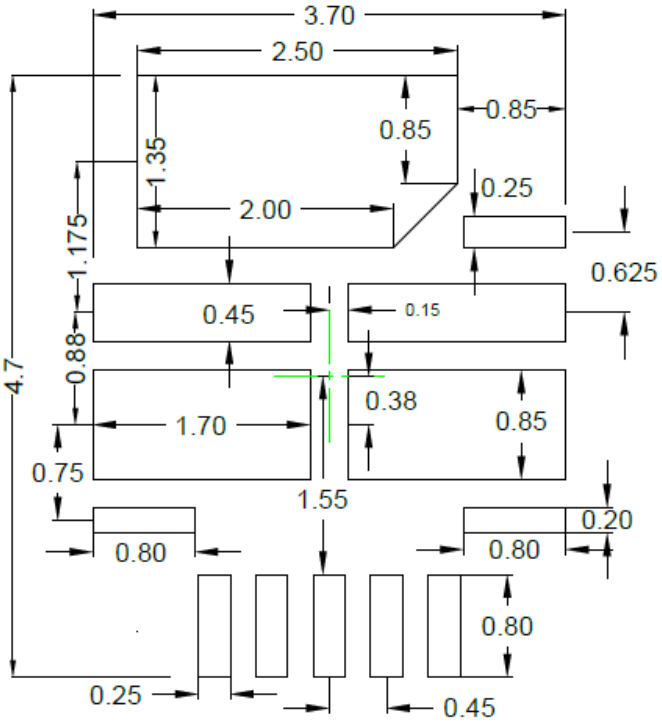
Top View



Bottom View



Front View

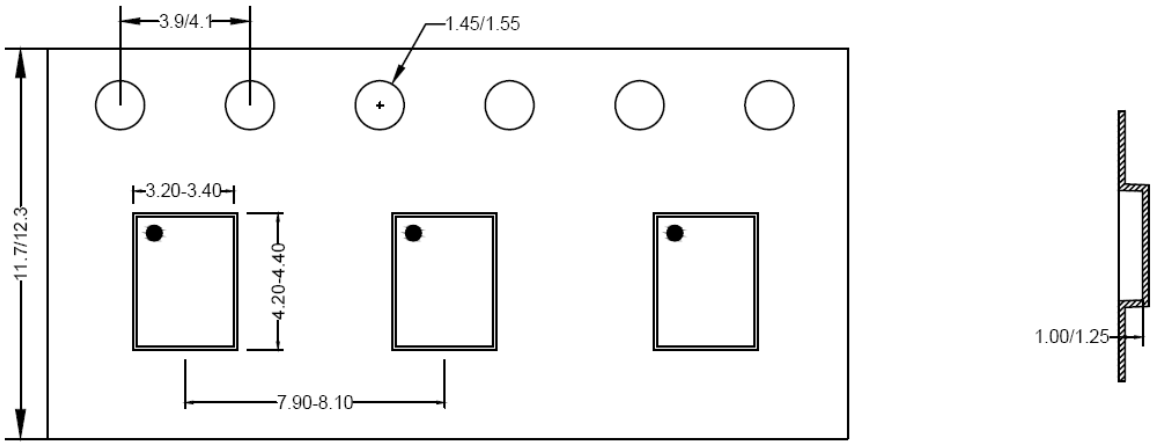


Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;
2, center line on drawing refers to the chip body center

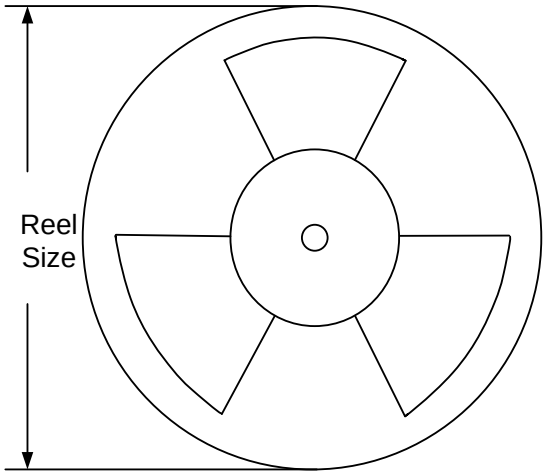
Taping & Reel Specification

1. QFN3×4-13 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

3. Others: NA