OR1401SBC

High Efficiency Fast Response, 1A, 27V Input Synchronous Step Down Regulator

General Description

OR1401SBC develops high efficiency synchronous step- down DC-DC converter capable of delivering 1A . OR1401SBC operates over a wide input voltage range from 4.5V to 27V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

OR1401SBC adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500 kHz under heavy load conditions to minimize the size of inductor and capacitor.

Ordering Information

OR1401□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
OR1401SBC	SOT23-6	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom):350/150 mΩ
- 4.5-27V Input Voltage Range
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- 2% 0.6V Reference
- RoHS Compliant and Halogen Free
- Compact Package: SOT23-6

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Typical Applications

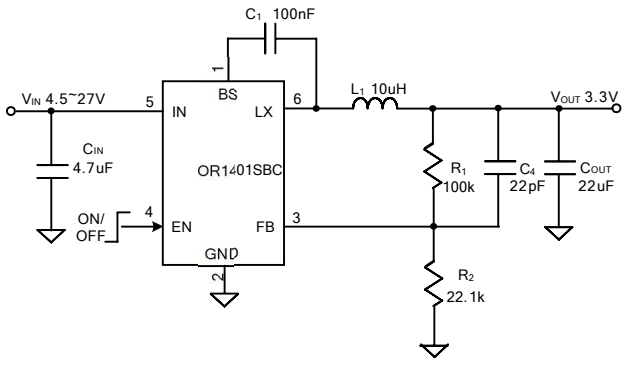


Figure 1. Schematic Diagram

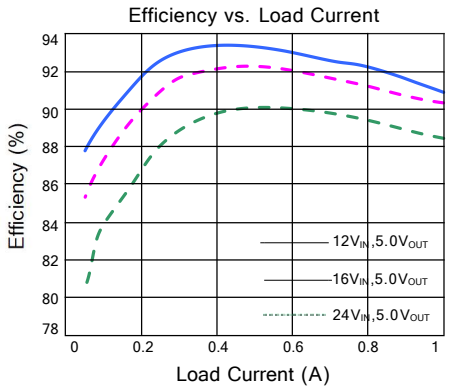
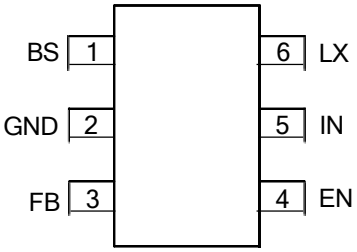


Figure 2. Efficiency vs Load Current

Pinout (top view)

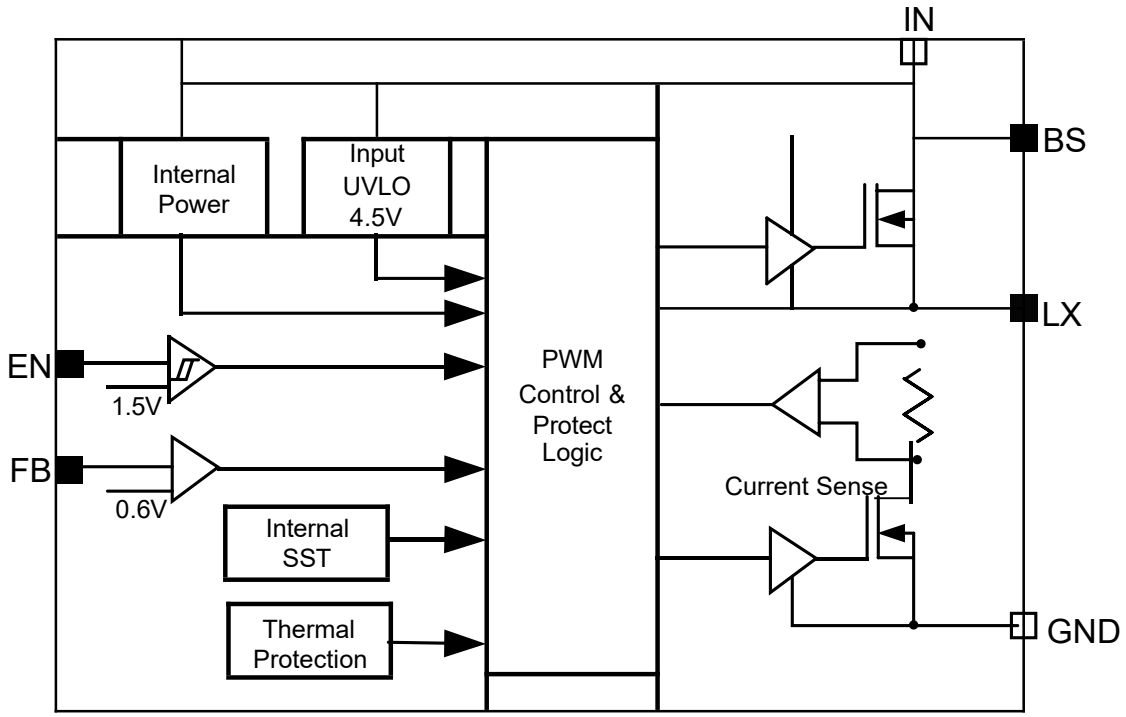


(SOT23-6)

Top Mark: **EN*xyz*, (**Device code: EN; ***x=year code, y=week code, z= lot number code*)

Pin Name	Pin Number	Pin Description
BS	1	Boot-Strap Pin. Supply high side gate driver. Decouple this pinto LX pin with 0.1uF ceramic cap.
GND	2	Ground pin
FB	3	Output Feedback Pin. Connect this pinto the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: Vout=0.6*(1+R1/R2)
EN	4	Enable control. Pull high to turn on. Do not float.
IN	5	Power input pin.
LX	6	Inductor pin. Connect this pinto the switching node of inductor

Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 30V
LX, EN Voltage---------- V_{IN} + 0.3V
FB, BS-LX Voltage---------- 4V
Power Dissipation, P_D @ T_A = 25°C SOT23-6, ---------- 0.6W
Package Thermal Resistance (Note 2)

θ_{JA} ---------- 170°C/W
θ_{JC} ---------- 130°C/W

Junction Temperature Range ---------- 125°C
Lead Temperature (Soldering, 10 sec.)---------- 260°C
Storage Temperature Range ----------65°C to 150°C
Dynamic LX voltage in 50ns duration ---------- IN+3V to GND-4V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.5V to 27V
Junction Temperature Range ---------- 40°C to 125°C
Ambient Temperature Range ----------40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.2uH, C_{OUT} = 10uF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

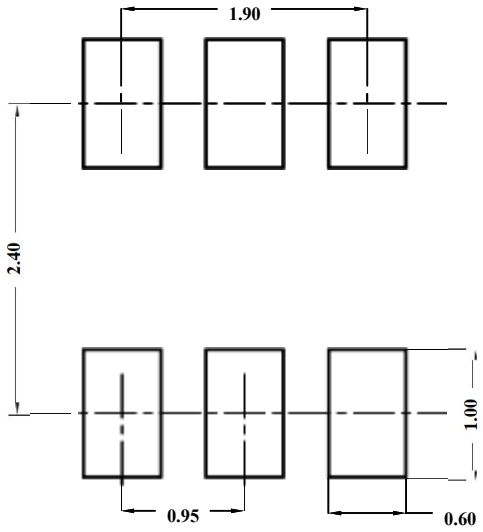
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		27	V
Quiescent Current	I_Q	$I_{OUT=0}$, $V_{FB}=V_{REF}\times105\%$		400		μA
Shutdown Current	I_{SHDN}	EN=0		5	10	μA
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
FB Input Current	I_{FB}	$V_{FB}=V_{IN}$	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			0.35		Ω
Bottom FET RON	$R_{DS(ON)2}$			0.15		Ω
Bottom FET Valley Current Limit	I_{LIM}		1.5			A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				4.5	V
UVLO Hysteresis	V_{HYS}			0.4		V
On Time	T_{ON}	V_{IN} = 12V ,V_{OUT}=1.2V, I_{OUT} = 1A		200		ns
Min ON Time				50		ns
Min Off Time				100		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

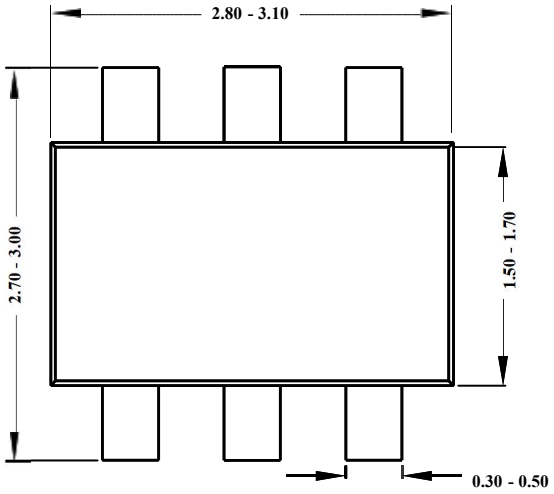
Note 2: θ JA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Pin 2 of SOT23-6 packages is the case position for θ JC measurement. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane

Note 3: The device is not guaranteed to function outside its operating conditions.

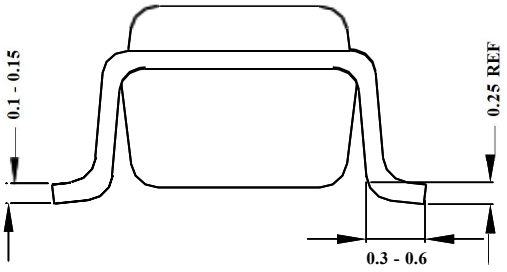
SOT23-6 Package Outline & PCB layout

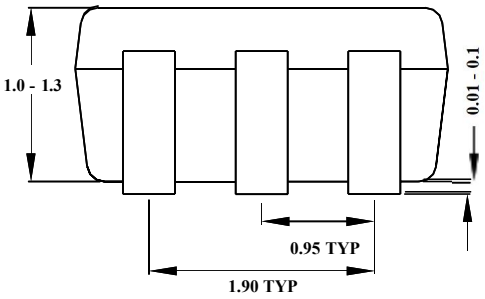


Recommended Pad Layout



Top View

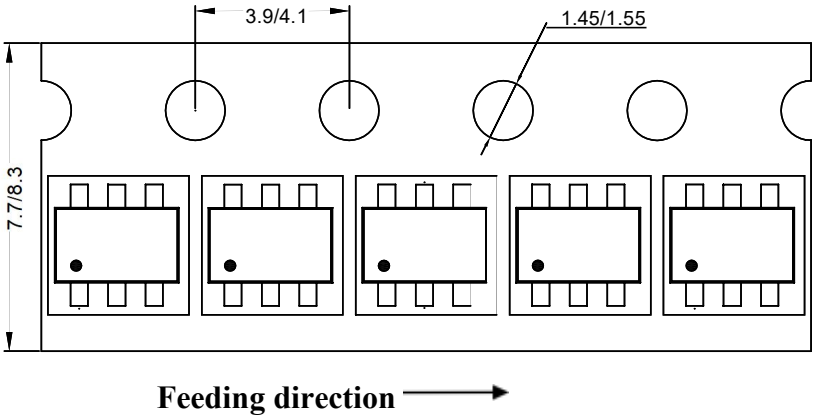




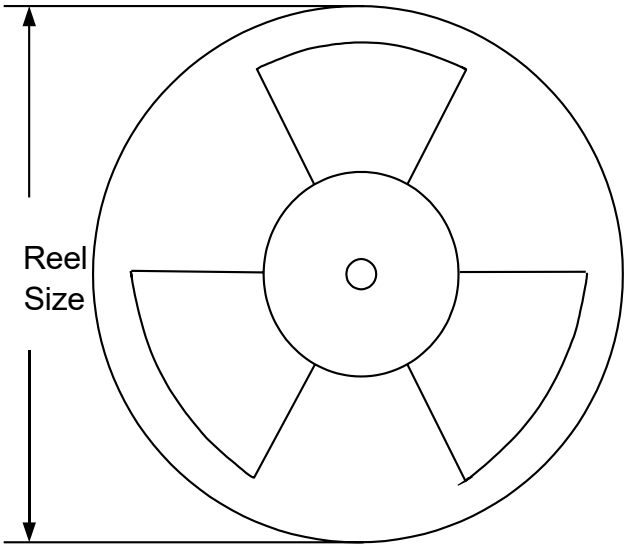
Notes: **All dimension in MM**
All dimension do not include mold flash & metal burr

Taping & Reel Specification

1. SOT23-6 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

3. Others: NA